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# Photodiode arrays with amplifiers

S13885-128/-256, S13886-128

## Photodiode arrays combined with signal processing IC for X-ray detection

The S13885-128/-256, S13886-128 are Si photodiode arrays combined with a signal processing IC chip. Improvement in the signal processing IC chip has achieved higher sensitivity compared to the previous products (S11865/S11866 series). The signal processing IC chip is formed by CMOS process and incorporates a timing generator, shift register, charge amplifier array, clamp circuit and hold circuit, making the external circuit configuration simple. A long and narrow image sensor can be configured by arranging multiple arrays in a row.

### Features

- **Data rate: 1 MHz max.**
- **Element pitch: 3 types available**
  **S13885-128: 0.4 mm pitch × 128 ch**
  **S13885-256: 0.2 mm pitch × 256 ch**
  **S13886-128: 0.8 mm pitch × 128 ch**
- **3.3 V power supply operation**
- **Simultaneous integration method by using a charge amplifier array**
- **Low dark current due to zero-bias photodiode operation**
- **Integrated clamp circuit allows low noise and wide dynamic range.**
- **Integrated timing generator allows operation at two different pulse timings.**
- **Detectable energy range: 30 k to 100 keV**
- **Types with phosphor sheet affixed on the photosensitive area are available for X-ray detection (S13885-128G/-256G, S13886-128G)**

### Applications

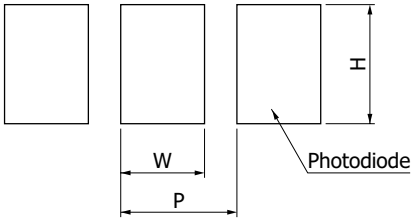
- **Line sensors for X-ray detection**
- **Long and narrow line sensors**

### Structure

| Parameter | Symbol*1 | S13885-128 | S13885-256 | S13886-128 | Unit |
|---|---|---|---|---|---|
| Element pitch | P | 0.4 | 0.2 | 0.8 | mm |
| Element width | W | 0.3 | 0.1 | 0.7 | mm |
| Element height | H | 0.6 | 0.3 | 0.8 | mm |
| Number of elements | - | 128 | 256 | 128 | - |
| Effective area length | - | 51.2 | 51.2 | 102.4 | mm |
| Board material | - | Glass epoxy | | | - |

*1: Refer to following figure.

### Enlarged drawing of photosensitive area



## Absolute maximum ratings (Ta=25 °C unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | Vdd | -0.3 to +4.2 | V |
| Reference voltage | Vref | -0.3 to +4.2 | V |
| Photodiode voltage | Vpd | -0.3 to +4.2 | V |
| Gain selection terminal voltage | Vgain | -0.3 to +4.2 | V |
| Master/slave selection voltage | Vms | -0.3 to +4.2 | V |
| Clock pulse voltage | V(CLK) | -0.3 to +4.2 | V |
| Reset pulse voltage | V(RESET) | -0.3 to +4.2 | V |
| External start pulse voltage | V(EXTSP) | -0.3 to +4.2 | V |
| Operating temperature*2 | Topr | -5 to +60 | °C |
| Storage temperature*2 | Tstg | -10 to +70 | °C |

*2: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

## Recommended terminal voltage (Ta=25 °C)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | Vdd | 3.0 | 3.3 | 3.6 | V |
| Reference voltage | | Vref | Vdd - 1.0 | Vdd - 0.8 | Vdd - 0.6 | V |
| Photodiode voltage | | Vpd | - | Vref | - | V |
| Gain selection terminal voltage | High gain | Vgain | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low gain | | 0 | - | 0.25 | V |
| Master/slave selection voltage | High level*3 | Vms | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level*4 | | 0 | - | 0.25 | V |
| Clock pulse voltage | High level | V(CLK) | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level | | 0 | - | 0.25 | V |
| Reset pulse voltage | High level | V(RESET) | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level | | 0 | - | 0.25 | V |
| External start pulse voltage | High level | V(EXTSP) | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level | | 0 | - | 0.25 | V |

*3: Parallel
*4: Serial at 2nd or later stages

## Electrical characteristics [Ta=25 °C, Vdd=3.3 V, V(CLK)=V(RESET)=3.3 V]

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse frequency*5 | | f(CLK) | 40 | - | 4000 | kHz |
| Line rate*6 | S13885/S13886-128 | LR | - | - | 7568 | lines/s |
| | S13885-256 | | - | - | 3844 | |
| Output impedance | | Zo | - | 3 | - | kΩ |
| Current consumption | S13885/S13886-128 | Ic | - | 36 | - | mA |
| | S13885-256 | | - | 72 | - | |
| Charge amplifier feedback capacitance | High gain | Cf | - | 0.125 | - | pF |
| | Low gain | | - | 0.25 | - | |

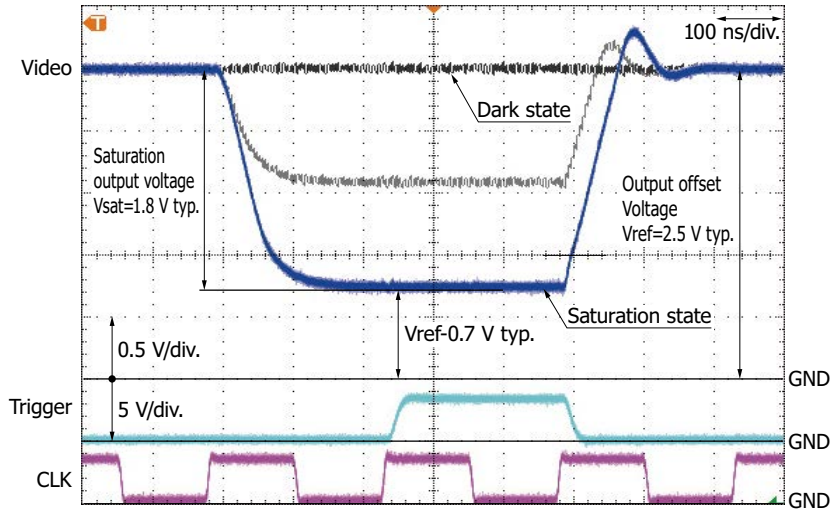
*5: Video data rate is 1/4 of f(CLK).
*6: The values depend on the clock pulse frequency.

## Electrical and optical characteristics [Ta=25 °C, Vdd=3.3 V, V(CLK)=V(RESET)=3.3 V, Vgain=3.3 V (high gain), 0 V (low gain)]

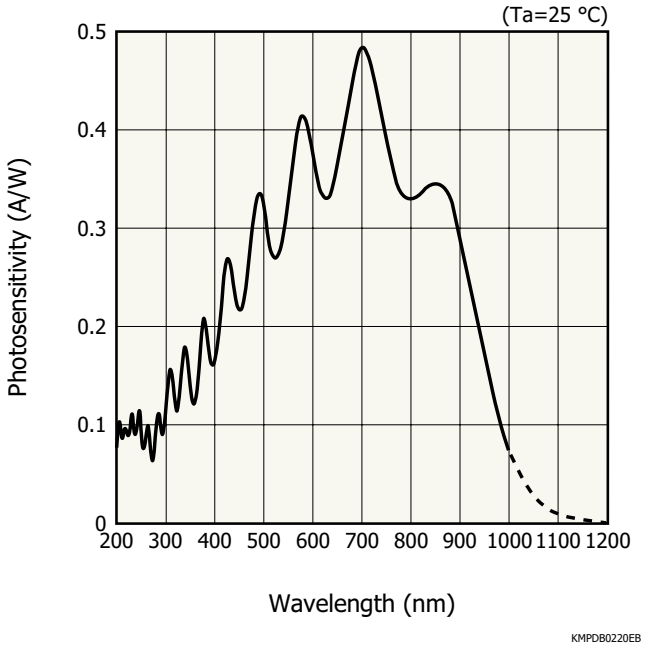
| Parameter | | Symbol | S13885-128G | | | S13885-256G | | | S13886-128G | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Spectral response range | | λ | 200 to 1000 | | | 200 to 1000 | | | 200 to 1000 | | | nm |
| Peak sensitivity wavelength*7 | | λp | - | 720 | - | - | 720 | - | - | 720 | - | nm |
| Dark output voltage*8 | High gain | VD | - | 0.02 | 0.2 | - | 0.02 | 0.2 | - | 0.02 | 0.2 | mV |
| | Low gain | | - | 0.01 | 0.1 | - | 0.01 | 0.1 | - | 0.01 | 0.1 | |
| Saturation output voltage | | Vsat | Vref - 1.0 | Vref - 0.7 | - | Vref - 1.0 | Vref - 0.7 | - | Vref - 1.0 | Vref - 0.7 | - | V |
| Saturation exposure*7 *9 | High gain | Pin_sat | - | 0.3 | 0.4 | - | 1.8 | 2.3 | - | 0.1 | 0.13 | m$lx$ · s |
| | Low gain | | - | 0.6 | 0.8 | - | 3.6 | 4.5 | - | 0.2 | 0.26 | |
| Photosensitivity*7 *9 | High gain | Sw | 4800 | 6000 | - | 800 | 1000 | - | 14080 | 17600 | - | V/$lx$ · s |
| | Low gain | | 2400 | 3000 | - | 400 | 500 | - | 7040 | 8800 | - | |
| Photoresponse nonuniformity*10 | | PRNU | - | - | ±10 | - | - | ±10 | - | - | ±10 | % |
| Readout noise*11 | High gain | Nread | - | 1.0 | 1.5 | - | 0.6 | 0.9 | - | 1.7 | 2.6 | mV rms |
| | Low gain | | - | 0.6 | 0.9 | - | 0.4 | 0.6 | - | 1.0 | 1.5 | |
| Output offset voltage*12 | | Voffset | - | Vref | - | - | Vref | - | - | Vref | - | V |

*7: Measured without phosphor sheet
*8: Integration time ts=1 ms
*9: Measured with a 2856 K tungsten lamp
*10: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the photosensitive area is uniformly illuminated by light which is approx. 50% of the saturation level. PRNU is defined as follows:
PRNU = ΔX/X × 100 [%]
X: average output of all elements, ΔX: difference between X and the maximum or minimum output, whichever is larger.
*11: Video data rate=1 MHz, dark state, ts=1 ms
*12: Video output is negative-going output with respect to the output offset voltage.

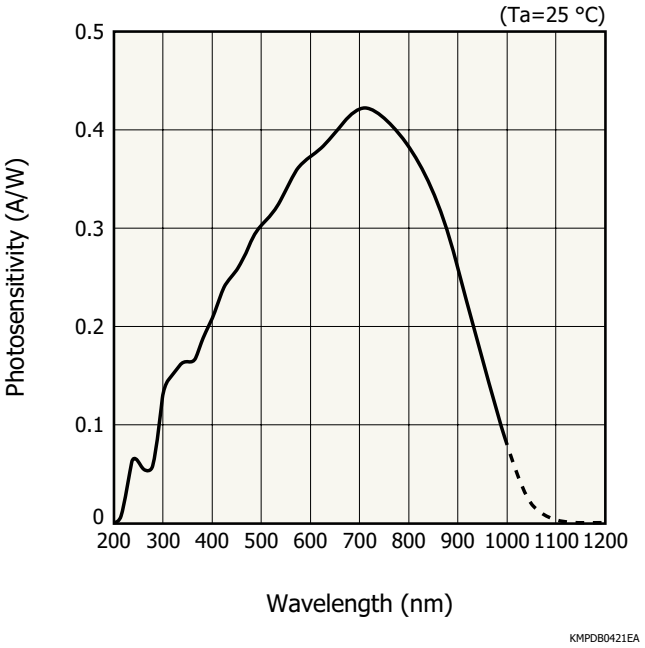
## Output waveform of one element



## Spectral response (typical example)

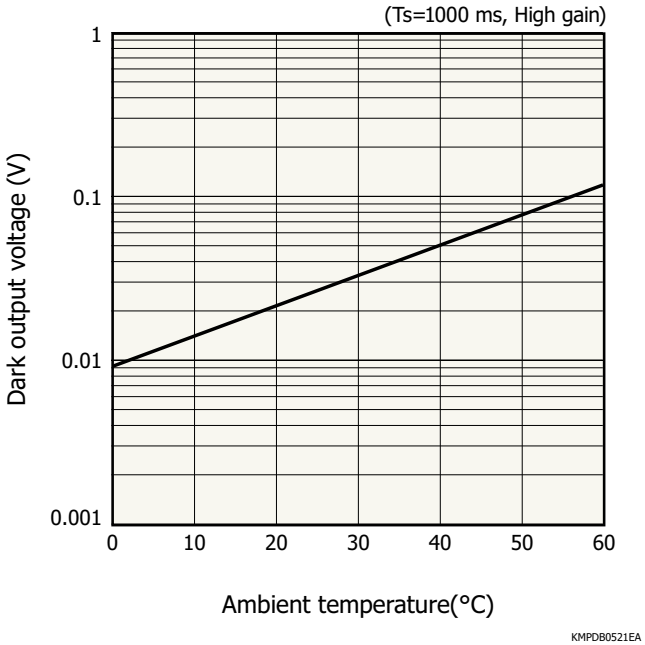



When silicone resin is applied (for attaching a fluorescent screen)



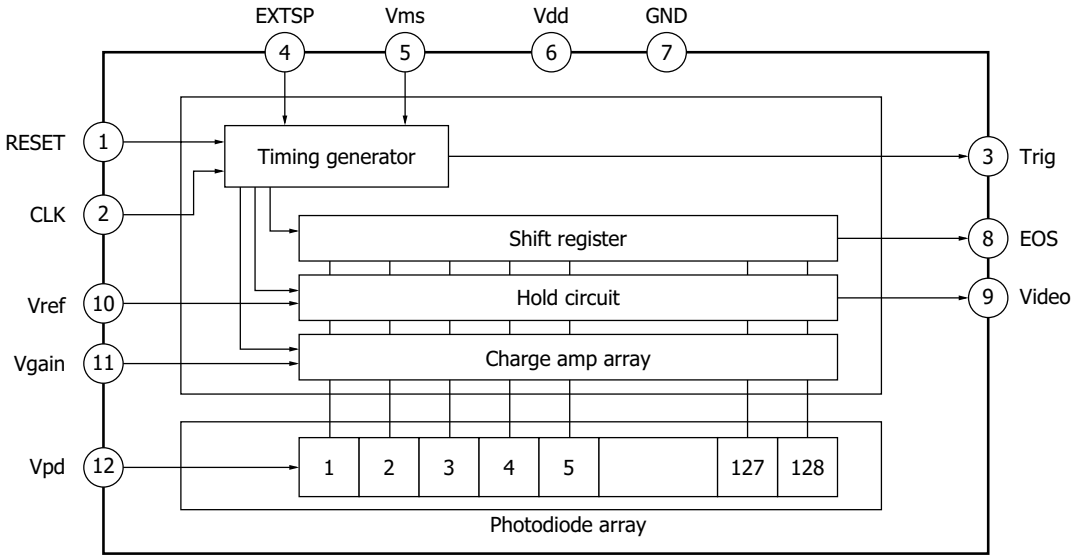

When the fluorescent screen is attached, the spectral response becomes smooth due to the effects of the adhesive resin.

## Dark output voltage vs. ambient temperature (typical example)



## Block diagram

S13885-128, S13886-128

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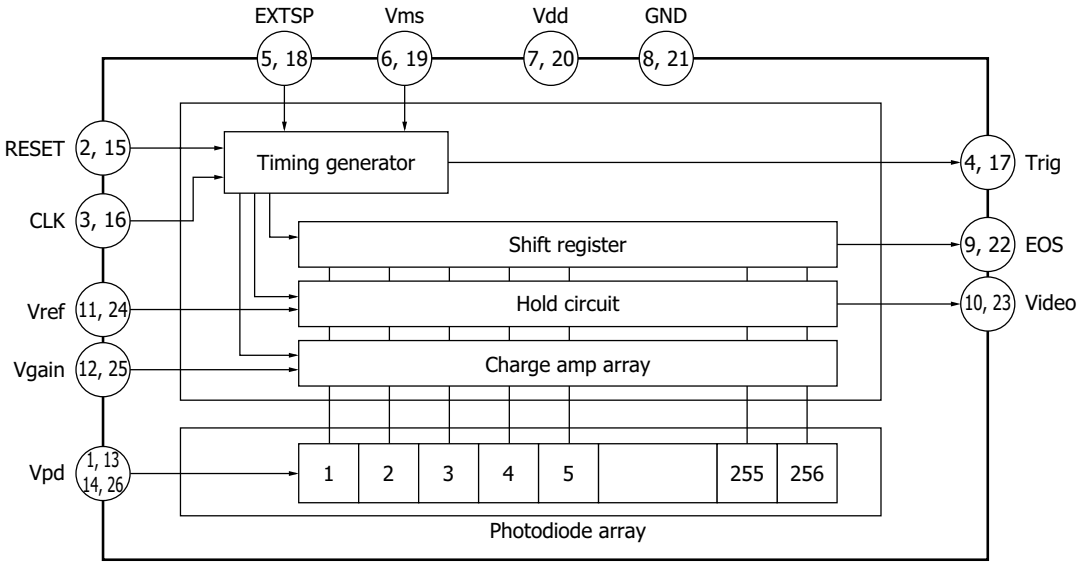
S13885-256

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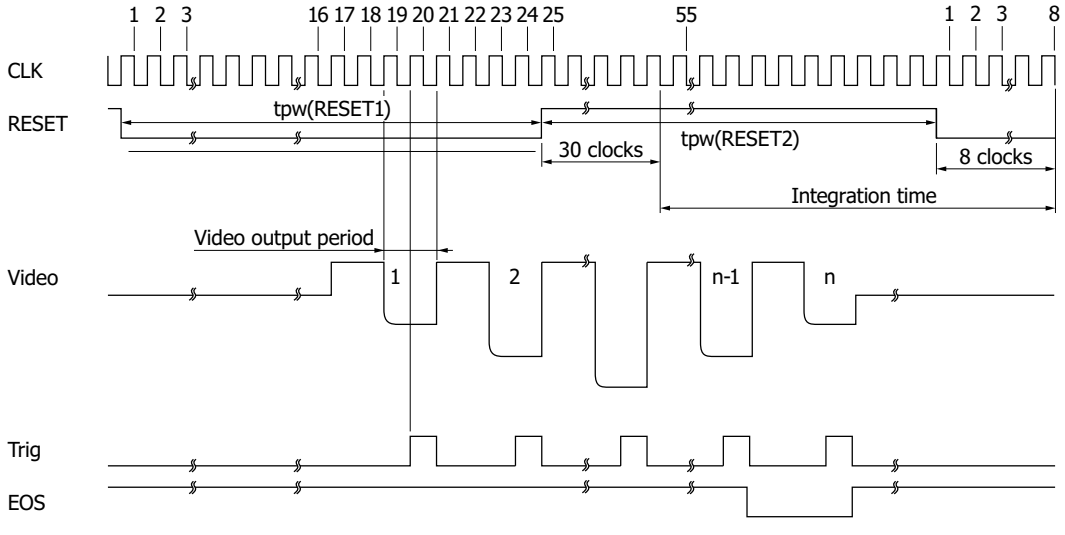
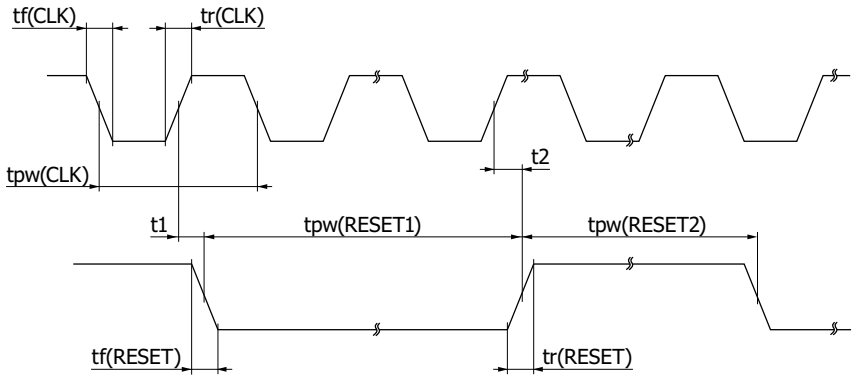
## Timing chart

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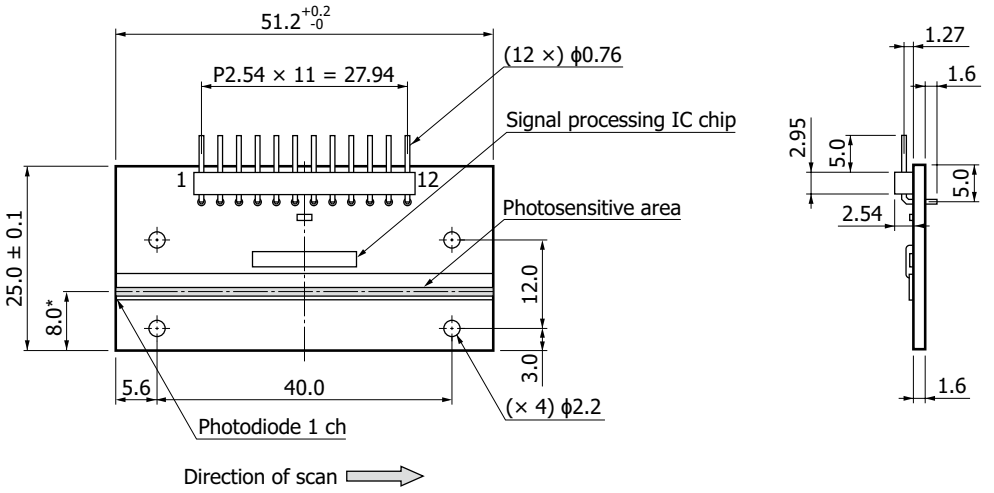
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock pulse width | tpw(CLK) | 250 | - | 25000 | ns |
| Clock pulse rise/fall times | tr(CLK), tf(CLK) | 0 | 20 | 30 | ns |
| Reset pulse width 1 | tpw(RESET1) | 25 | - | - | CLK |
| Reset pulse width 2 | tpw(RESET2) | 40 | - | - | CLK |
| Reset pulse rise/fall times | tr(RESET), tf(RESET) | 0 | 20 | 30 | ns |
| Clock pulse-reset pulse timing 1 | t1 | -20 | 0 | 20 | ns |
| Clock pulse-reset pulse timing 2 | t2 | -20 | 0 | 20 | ns |

1. The internal timing circuit starts operation at the falling edge of CLK immediately after a RESET pulse goes low.
2. When the falling edge of this CLK is counted as 1 clock, the video signal of the 1st channel appears between 18.5 clocks and 20.5 clocks. Subsequent video signals appear every 4 clocks.
3. The trigger pulse for the 1st channel rises at a timing of 19.5 clocks and then rises every 4 clocks. The rising edge of each trigger pulse is the recommended timing for data acquisition.
4. Signal charge integration time equals [the high period of a RESET pulse - 22 clocks]. The charge integration starts at the fall of the 30th clock after the rise of the RESET pulse and ends at the fall of the 8th clock after the fall of the RESET pulse. After the RESET pulse next changes from high to low, signals integrated within this period are sequentially read out as time-series signals by the shift register operation. The rise and fall of a RESET pulse must be synchronized with the rise of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to [16.5 + 4 × N (number of elements)] clocks.
5. The video signal after an EOS signal output becomes a high impedance state, and the video output will be indefinite.

## Dimensional outlines (unit: mm)

S13885-128




Tolerance unless otherwise noted: ±0.2
* Distance from board bottom to photosensitive area center
Board: G10 glass epoxy
Connector: PRECI-DIP DURTAL 800-10-012-20-001101

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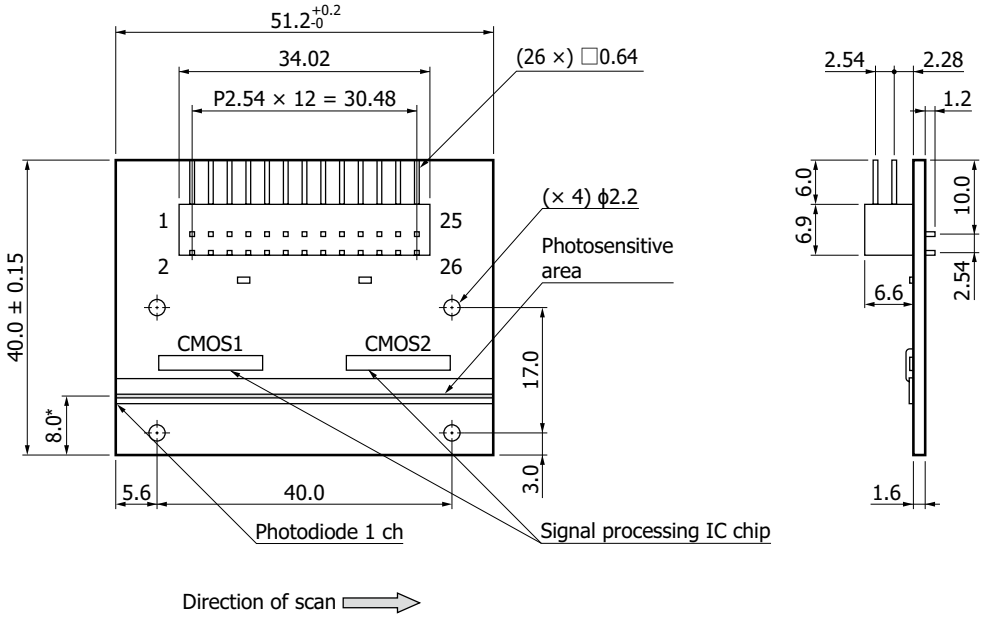
S13885-256




Tolerance unless otherwise noted: ±0.2
* Distance from board bottom to photosensitive area center
Board: G10 glass epoxy
Connector: JAE (Japan Aviation Electronics Industry, Limited) PS-26PE-D4LT1-PN1

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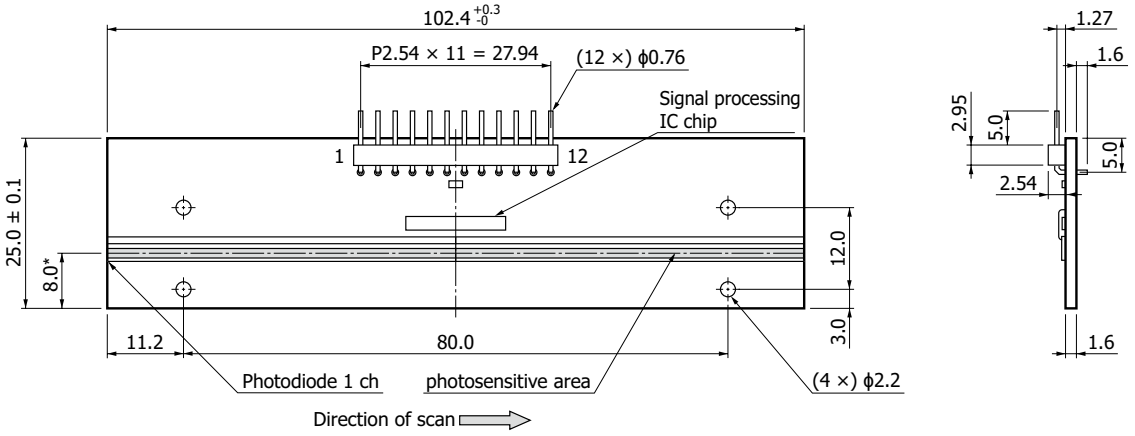
## S13886-128




Tolerance unless otherwise noted: ±0.2
* Distance from board bottom to photosensitive area center
Board: G10 glass epoxy
Connector: PRECI-DIP DURTAL 800-10-012-20-001101

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## Pin connections

S13885-128, S13886-128

| Pin no. | Symbol | Name | Note |
|---|---|---|---|
| 1 | RESET | Reset pulse | Pulse input |
| 2 | CLK | Clock pulse | Pulse input |
| 3 | Trig | Trigger pulse | Positive-going pulse output |
| 4 | EXTSP | External start pulse | Pulse input |
| 5 | Vms | Master/slave selection voltage | Voltage input |
| 6 | Vdd | Supply voltage | Voltage input |
| 7 | GND | Ground | |
| 8 | EOS | End of scan | Negative-going pulse output |
| 9 | Video | Video output | Negative-going output from Vref |
| 10 | Vref | Reference voltage | Voltage input |
| 11 | Vgain | Gain selection terminal voltage | Voltage input |
| 12 | Vpd | Photodiode voltage | Voltage input |

S13885-256

| Pin no. | CMOS1 | Pin no. | CMOS2 | Name | Note |
|---|---|---|---|---|---|
| 1 | Vpd | 14 | Vpd | Photodiode voltage | Voltage input |
| 2 | RESET | 15 | RESET | Reset pulse | Pulse input |
| 3 | CLK | 16 | CLK | Clock pulse | Pulse input |
| 4 | Trig | 17 | Trig | Trigger pulse | Positive-going pulse output |
| 5 | EXTSP | 18 | EXTSP | External start pulse | Pulse input |
| 6 | Vms | 19 | Vms | Master/slave selection voltage | Voltage input |
| 7 | Vdd | 20 | Vdd | Supply voltage | Voltage input |
| 8 | GND | 21 | GND | Ground | |
| 9 | EOS | 22 | EOS | End of scan | Negative-going pulse output |
| 10 | Video | 23 | Video | Video output | Negative-going output from Vref |
| 11 | Vref | 24 | Vref | Reference voltage | Voltage input |
| 12 | Vgain | 25 | Vgain | Gain selection voltage | Voltage input |
| 13 | Vpd | 26 | Vpd | Photodiode voltage | Voltage input |

## Gain selection terminal voltage setting

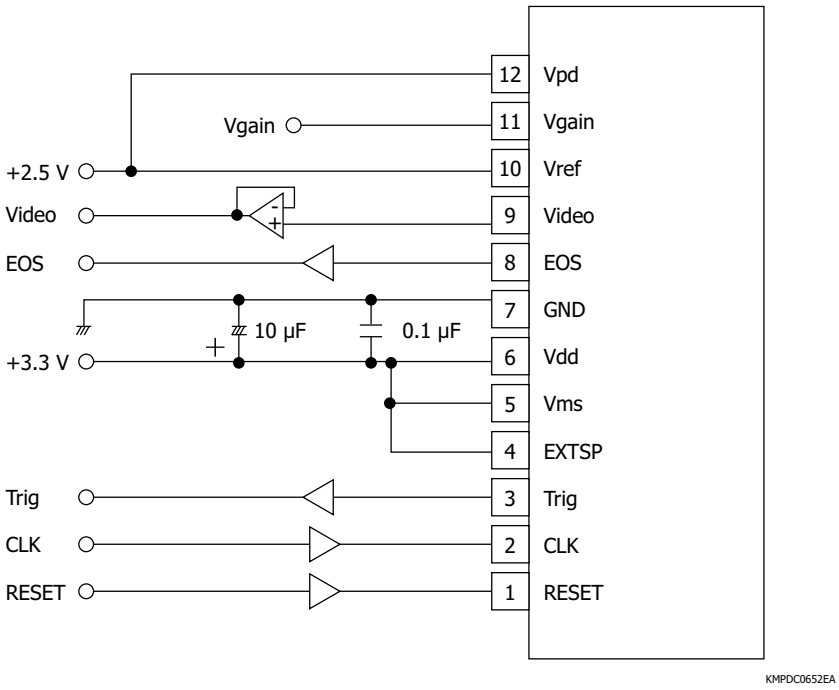
Vdd: High gain (Cf=0.125 pF) GND: Low gain (Cf=0.25 pF)

## Setting for each readout method

| S13885-128, S13886-128 |
|---|

Set to A in the table below in most cases.
To serially read out signals from two or more sensors linearly connected, set the 1st sensor to A and the 2nd or later sensors to B.
The CLK and RESET pulses should be shared with each sensor and the video output terminal of each sensor connected together.

■ Connection example (parallel readout)




Note: When making a serial connection with two or more sensors or when connecting the sensor with a long cable, connect a high-impedance amplifier near the sensor if necessary.

| Setting | Readout method | Vms | EXTSP |
|---|---|---|---|
| A | All stages of parallel readout, serial readout at 1st sensor | Vdd | Vdd |
| B | Serial readout at 2nd and later sensors | GND | Preceding sensor EOS is input. |

S13885-256

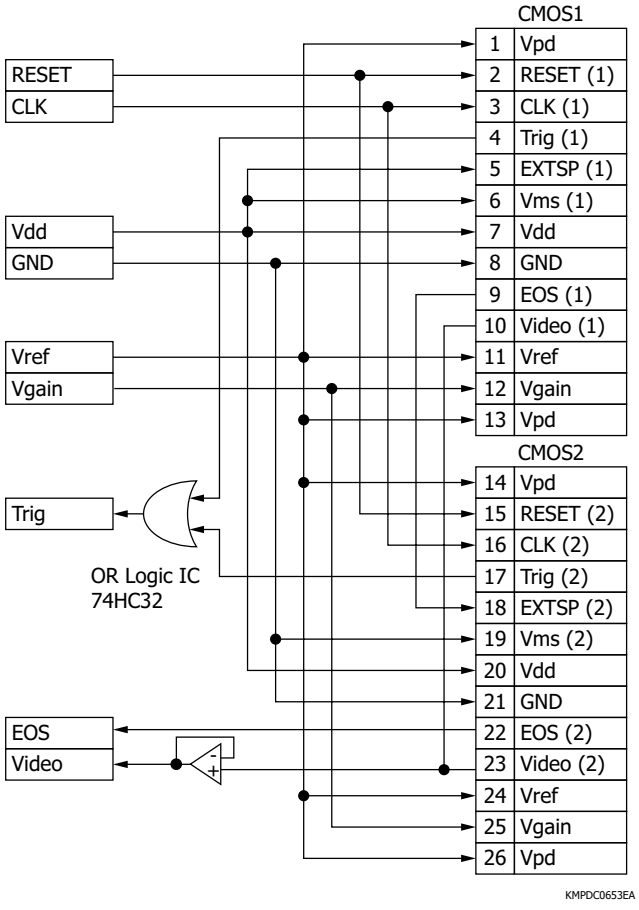
Signals of channels 1 through 128 are output from CMOS1, while signals of channels 129 through 256 are output from CMOS2. The following two readout methods are available.

(1) Serial readout method
CMOS1 and CMOS2 are connected in serial and the signals of channels 1 through 256 are sequentially read out from one output line. Set CMOS1 as in "A" in the table below, and set CMOS2 as in "B". Use a common CLK for CMOS1 and CMOS2. Likewise, use a common RESET for CMOS1 and CMOS2. Connect the video output terminals to a single line.

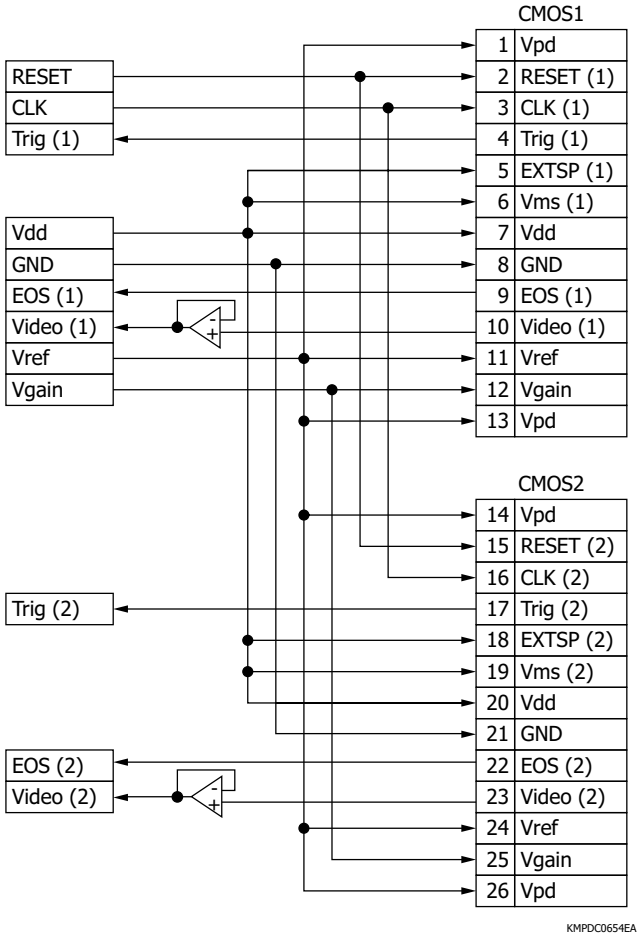
(2) Parallel readout method
128 channel signals are output in parallel respectively from the output lines of CMOS1 and CMOS2. Set both CMOS1 and CMOS2 as in "A" in the table below.

■ Connection examples

• Serial readout method




• Parallel readout method




Note: When making a serial connection with two or more sensors or when connecting the sensor with a long cable, connect a high-impedance amplifier near the sensor if necessary.

| Setting | Vms | EXTSP |
|---|---|---|
| A | Vdd | Vdd |
| B | GND | Preceding sensor EOS is input. |

## Readout circuit

Apply pulse signals that meet the required conditions to the input terminals. Video output should be amplified by an op amp that is connected close to the sensor.

## Precautions

(1) The signal processing IC chip is protected against static electricity. However, in order to prevent possible damage to the IC chip, take electrostatic countermeasures such as grounding yourself, as well as workbench and tools. Also protect the IC chip from surge voltages from peripheral equipment.

(2) Gold wires for wire bonding are very thin, so they easily break if subjected to mechanical stress. The signal processing IC chip and wire bonding are covered with resin for protection, but make sure they do not get scratched.
Never touch these portions or the photodiode array chip affixed with the phosphor sheet. Excessive force, if applied, may break the wires or cause malfunction. Blow air to remove dust or debris if it gets on the protective resin. Never wash them with solvent. Signals may not be obtained if dust or debris is left or a scratch is made on the protective resin or the phosphor sheet or if the signal processing IC chip or photodiode array chip is nicked.

(3) The photodiode array characteristics may deteriorate when operated at high humidity, so put it in a hermetically sealed enclosure or case. When installing the photodiode array with amplifier on a board, be careful not to cause the board to warp.

(4) The characteristics of the signal processing IC chip deteriorate if exposed to X-rays. So use a lead shield which is at least 1 mm larger all around than the signal processing IC chip. The 1 mm margin may not be sufficient depending on the incident angle of X-rays. Provide an even larger shield as long as it does not cover the photodiode photosensitive area. Since the optimal shield thickness depends on the operating conditions, calculate it by taking the attenuation coefficient of lead into account.

(5) The sensitivity of the photodiode array chip decreases if continuously exposed to X-rays. The extent of this sensitivity decrease differs depending on the X-ray irradiation conditions.

(6) When a scintillator is mounted on a photodiode array chip, increased photoresponse nonuniformity caused by the intrusion of bubbles due to adhesive resin shortage is a concern. Make sure that the adhesive resin covers the entire photodiode array chip.
The photodiode array chip is hard but at the same time fragile and easily chipped. When mounting a scintillator on a photodiode array chip, be careful not to physically damage the chip with a sharp object or the like.

## Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Unsealed products
· Image sensors



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