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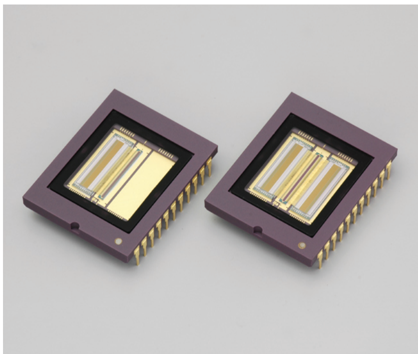
NEW

InGaAs linear image sensors



G11608 series

Wide spectral response range, near infrared image sensors (0.5 to 1.7 μm)

The G11608 series InGaAs linear image sensors are specifically designed for near infrared multichannel spectrophotometry. The G11608 series consists of an InGaAs photodiode array with enhanced sensitivity at shorter wavelengths, and CMOS chip that contains a charge amplifier array, a shift register, and a timing generator. The charge amplifier array is made up of CMOS transistors connected to each pixel of the InGaAs photodiode array. Signals from each pixel are read out in charge integration mode to achieve high sensitivity and stable operation.
The signal processing circuit on the CMOS chip offers two levels of conversion efficiency (CE) that can be selected by the external voltage to meet the application.

Features

- **Wide spectral response range (0.5 to 1.7 μm)**
- **Low noise**
- **Two selectable conversion efficiencies**
- **Anti-saturation circuit**
- **CDS (correlated double sampling) circuit*1**
- **Built-in thermistor**
- **Simple operation (by built-in timing generator)*2**
- **High resolution: 25 μm pitch (G11608-512DA)**

Applications

- **Near infrared multichannel spectrophotometry**
- **Radiation thermometry**
- **Non-destructive inspection**

*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS (correlated double sampling) circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.
*2: Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (programmable logic device) are used to input the required timing signals. However, the G11608 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

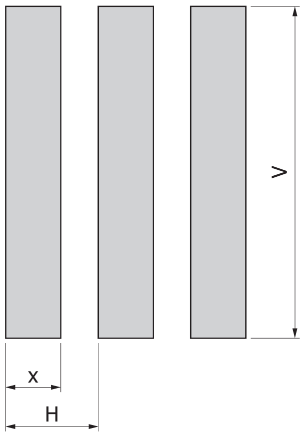
Selection guide

Type no.	Cooling	Image area (mm)	Number of total pixels	Number of effective pixels
G11608-256DA	Non-cooled	12.8 × 0.50	256	256
G11608-512DA			512	512

Structure

Type no.	Pixel size [μm (H) × μm (V)]	Pixel pitch (μm)	Package	Window material
G11608-256DA	50 × 500	50	22-pin ceramic	Borosilicate glass without anti-reflective coating
G11608-512DA	25 × 500	25		

Details of photosensitive area (unit: μm)



Number of pixels	x	H	V
256	30	50	500
512	10	25	500

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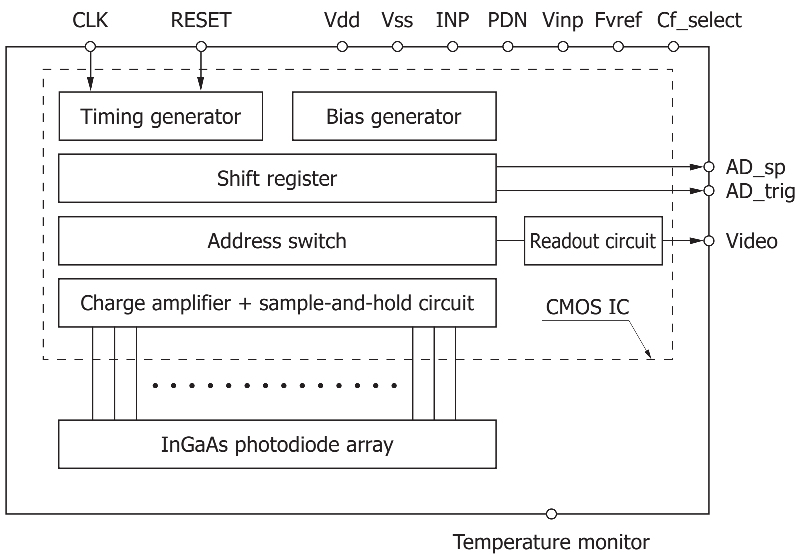
Block diagram



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Absolute maximum ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vdd, INP, Fvref Vinp, PDN	Ta=25 °C	-0.3	-	+6	V
Clock pulse voltage	Vϕ	Ta=25 °C	-0.3	-	+6	V
Reset pulse voltage	V(RES)	Ta=25 °C	-0.3	-	+6	V
Gain selection terminal voltage	Vcfsel	Ta=25 °C	-0.3	-	+6	V
Operating temperature*3	Topr	Non dew condensation	-10	-	+60	°C
Storage temperature*3	Tstg	Non dew condensation	-20	-	+70	°C
Soldering conditions	-		260 °C or less, within 5 s			-
Thermistor power dispation	Pth		-	-	400	mW

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.7	5.0	5.3	V
Differential reference voltage		Fvref	1.1	1.2	1.3	V
Video line reset voltage		Vinp	3.9	4.0	4.1	V
Input stage amplifier reference voltage		INP	3.9	4.0	4.1	V
Photodiode cathode voltage		PDN	3.9	4.0	4.1	V
Ground		GND	-	0	-	V
Clock pulse voltage	High	Vϕ	4.7	5.0	5.3	V
	Low		0	0	0.4	
Reset pulse voltage	High	V(RES)	4.7	5.0	5.3	V
	Low		0	0	0.3	

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Consumption current	G11608-512DA	I(Vdd)	-	45	80	mA
	G11608-256DA		-	85	120	
		Ifvref	-	-	1	mA
		Ivinp	-	-	1	mA
		Iinp	-	-	1	mA
		Ipdn	-	-	1	mA
Operation frequency		fop	0.1	1	5	MHz
Video data rate		DR	0.1	f	5	MHz
Video output voltage	High	VH	-	4.0	-	V
	Low	VL	-	1.2	-	V
Output offset voltage		Vos	-	Fvref	-	V
Output impedance		Zo	-	5	-	kΩ
AD_trig, AD_sp pulse voltage	High	Vtrig, Vsp	-	Vdd	-	V
	Low		-	GND	-	
Thermistor resistance		Rth	9.0	10.0	11.0	kΩ
Thermistor B constant*4		B	-	3950	-	K

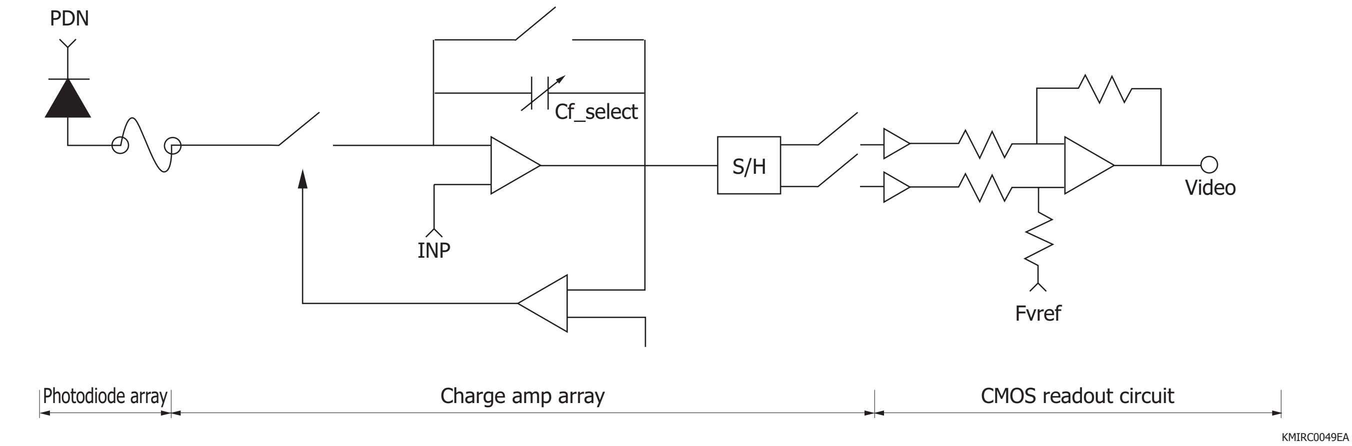
*4: T_1=25 °C, T_2=50 °C

Electrical and optical characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vϕ=5 V, f=1 MHz)

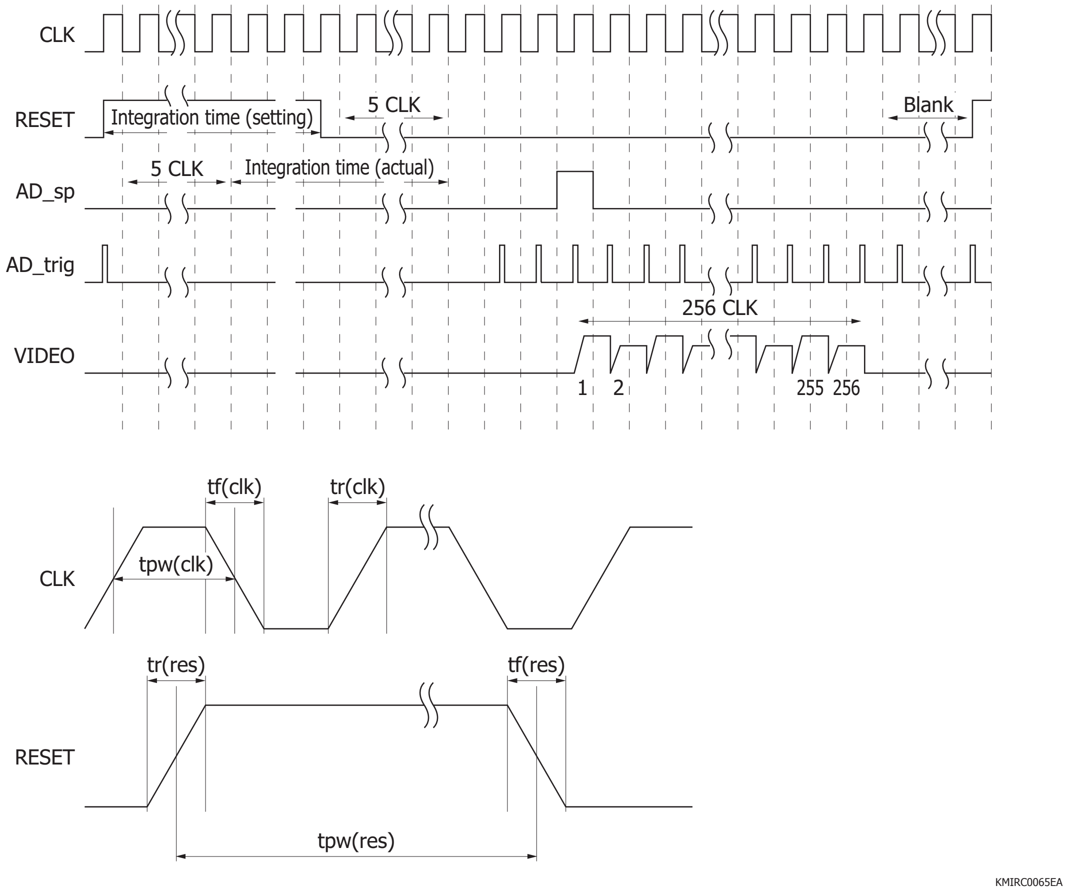
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range		λ		-	0.5 to 1.7	-	µm
Peak sensitivity wavelength		λp		-	1.55	-	µm
Photo sensitivity		S	λ=λp	0.8	1.0	-	A/W
Conversion efficiency*5		CE	Cf=10 pF	-	16	-	nV/e^-
			Cf=1 pF	-	160	-	
Photoresponse nonuniformity*6		PRNU		-	±3	±5	%
Saturation charge		Qsat	CE=16 nV/e^-	168	175	-	Me^-
			CE=160 nV/e^-	16.8	17.5	-	
Saturation voltage		Vsat		2.7	2.8	-	V
Dark output	G11608-256DA	V_D	CE=16 nV/e^-	-1	±0.1	1	V/s
	G11608-512DA			-0.5	±0.05	0.5	
Dark current	G11608-256DA	I_D	CE=16 nV/e^-	-10	±1	10	pA
	G11608-512DA			-5	±0.5	5	
Temperature coefficient of dark output (dark current)		-	CE=16 nV/e^-	-	1.1	-	times/°C
Readout noise*7		N	CE=16 nV/e^-	-	200	400	µVrms
			CE=160 nV/e^-	-	300	500	
Dynamic range		D	CE=16 nV/e^-	6750	14000	-	-
Defective pixels*8		-	CE=16 nV/e^-	-	-	1	%

*5: Refer to pin connection when changing conversion efficiency.
*6: 50% of saturation, integration time 10 ms, after dark output subtraction, excluding first and last pixels
*7: Integration time=10 ms (CE=16nV/e^-), 1 ms (CE=160 nV/e^-)
*8: Pixels with photoresponse nonuniformity, readout noise, or dark current higher than the maximum value

Equivalent circuit

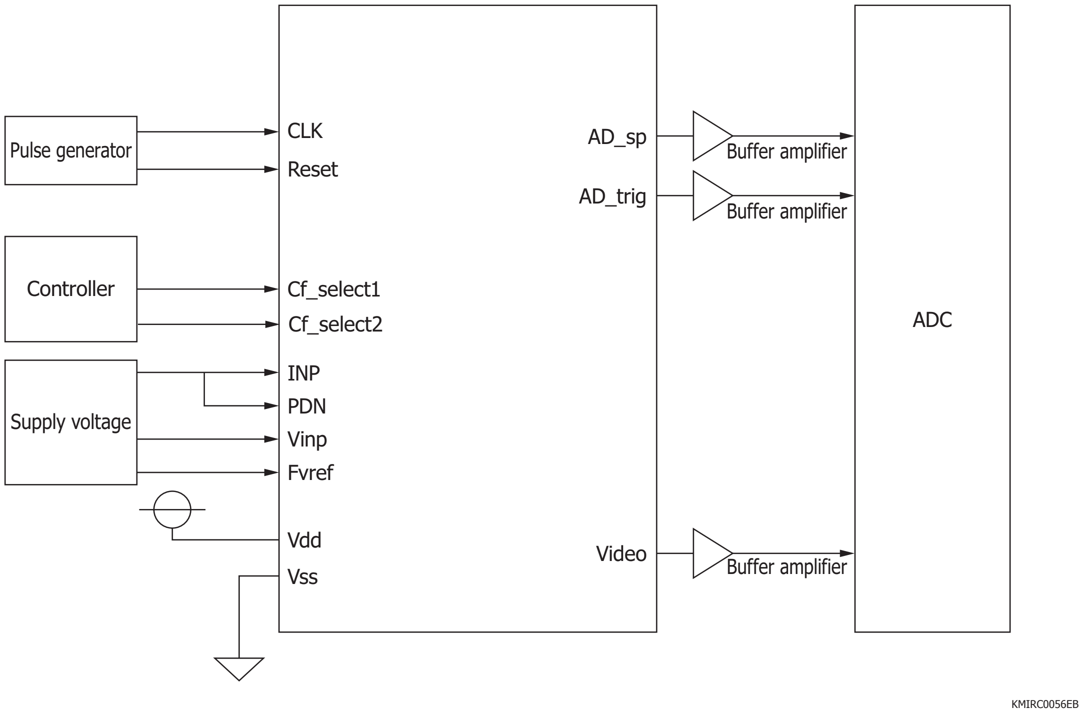


Timing chart (each video line)

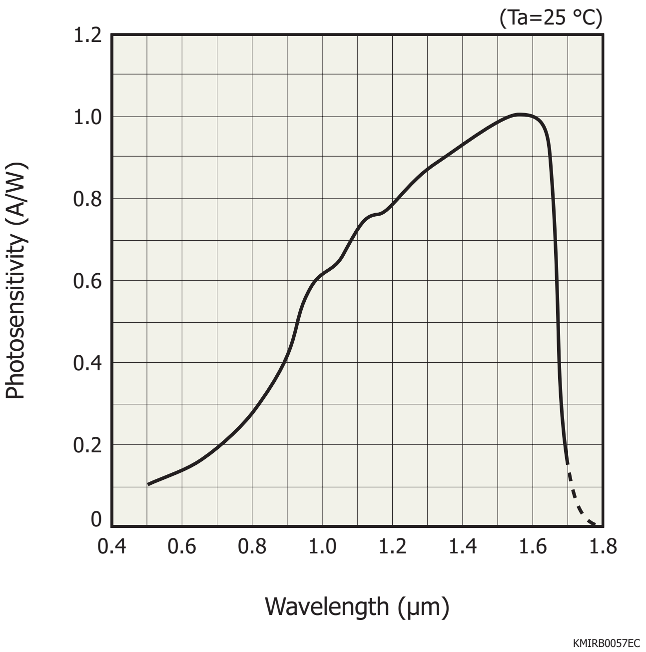


Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse width		tpw(clk)	60	500	5000	ns
Clock pulse rise/fall times		tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	High	tpw(res)	6	-	-	clocks
	Low		284	-	-	
Reset pulse rise/fall times		tr(res), tf(res)	0	20	30	ns

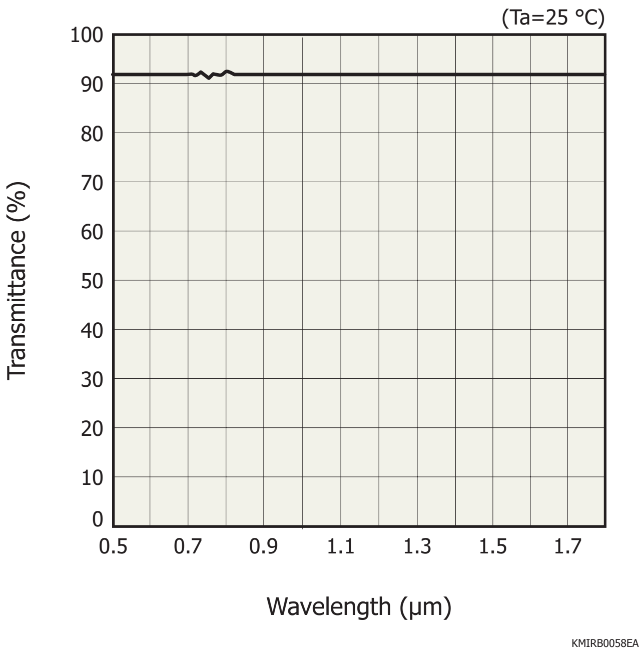
Connection example



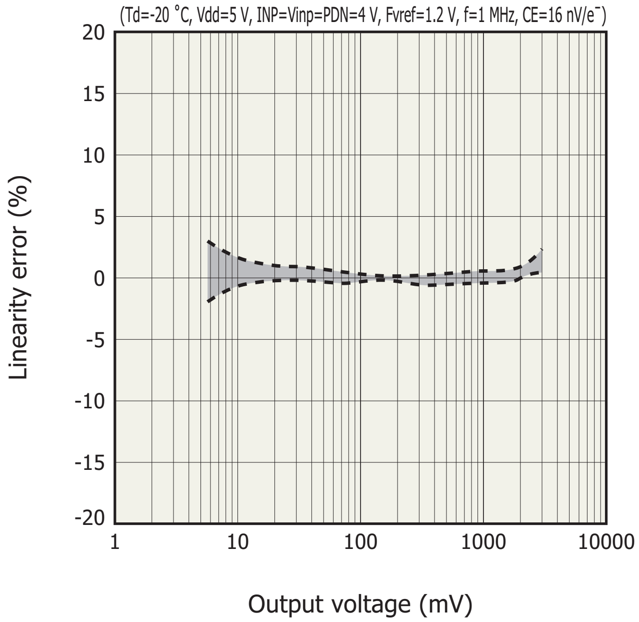
Spectral response (typical example)



Spectral transmittance characteristic of window material (typical example)



Linearity error



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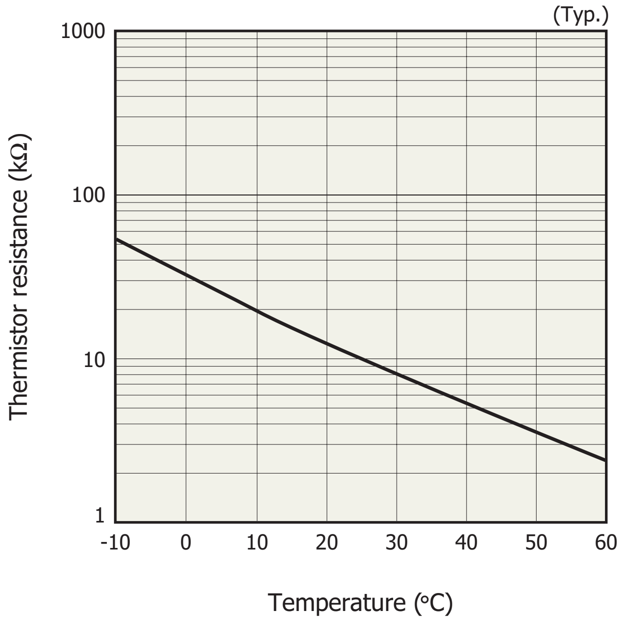
Temperature characteristics of thermistor



(Typ.)

Temperature (°C)	Thermistor resistance (kΩ)
-10	53.0
-5	41.2
0	32.1
5	25.1
10	19.8
15	15.7
20	12.5
25	10.0
30	8.06
35	6.53
40	5.32
45	4.36
50	3.59
55	2.97
60	2.47

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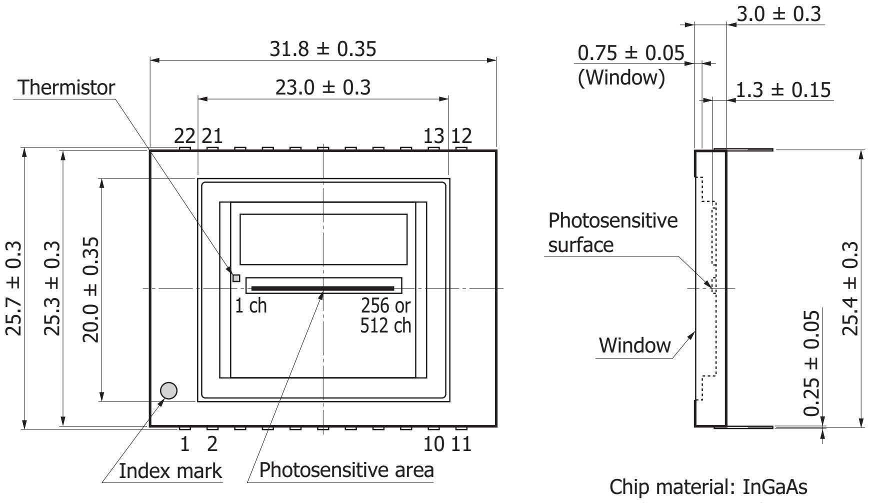
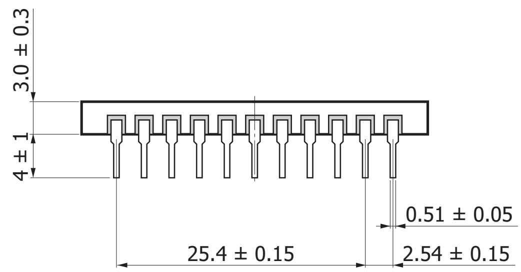
Dimensional outline (unit: mm)





Pin no.	G11608-256DA	G11608-512DA
1	NC	AD_sp_EVEN
2	NC	RESET_EVEN
3	NC	AD_trig_EVEN
4	NC	NC
5	Cf_select2	Cf_select2
6	Cf_select1	Cf_select1
7	Thermistor	Thermistor
8	Thermistor	Thermistor
9	NC	CLK_EVEN
10	Fvref	Fvref
11	NC	VIDEO_EVEN
12	VIDEO	VIDEO_ODD
13	Vinp	Vinp
14	CLK	CLK_ODD
15	PDN*	PDN*
16	INP*	INP*
17	GND	GND
18	Vdd	Vdd
19	NC	NC
20	AD_trig	AD_trig_ODD
21	RESET	RESET_ODD
22	AD_sp	AD_sp_ODD

* PDN and INP should be at the same potential. It is recommended to use the same power source and short between their pins

Chip material: InGaAs
Package material: ceramic
Lead treatment: Ni/Au plating
Lead material: FeNi alloy
Window material: borosilicate glass
Reflective index of window material: nd=1.47
Window material thickness: 0.75 ± 0.05 mm
AR coat: none
Window sealing method: resin adhesion
Position accuracy of photosensitive area center: ±0.3 (with respect to package center)
Rotation accuracy of photosensitive area: ±5 ° (with respect to package center)

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Pin connections

Terminal name	Input/Output	Function and recommended connection	Remark
PDN	Input	Cathode bias terminal for InGaAs photodiode. This should be at the same potential as INP.	4.0 V
AD_sp	Output	Digital start signal for A/D conversion	0 to 5 V
Cf_select1, 2	Input*8	Signal for selecting feedback capacitance (integration capacitance) on CMOS chip	0 V or 5 V
Thermistor	Output	Thermistor for minitoring temperature inside the package	-
AD_trig	Output	Sampling synchronous signal for A/D conversion	0 to 5 V
RESET	Input	Reset pulse for initializing the feedback capacitance in the charge amplifier formed in the CMOS chip. Integration time is determined by the high period of this pulse.	0 to 5 V
CLK	Input	Clock pulse for operating the CMOS shift register	0 to 5 V
INP	Input	Input stage amplifier reference voltage. Supply voltage for operating the signal processing circuit in the CMOS chip. This should be at the same potential as PDN.	4.0 V
Vinp	Input	Video line reset voltage. Supply voltage for operating the signal processing circuit in the CMOS chip.	4.0 V
Fvref	Input	Differential amplifier reference voltage. Supply voltage for operating the signal processing circuit in the CMOS chip.	1.2 V
VIDEO	Output	Differential amplifier output. Analog video signal.	1.2 to 3.0 V
Vdd	Input	Supply voltage for operating the signal processing circuit in the CMOS chip (+5 V)	5 V
GND	Input	Grand for the signal processing circuit in the CMOS chip (0 V)	0 V

*8: Conversion efficiency is determined by supply voltage to the Cf_select terminals as shown below.

Conversion efficiency	Cf_select1	Cf_select2
16 nV/e$^-$ (Cf=10 pF)	High	High
160 nV/e$^-$ (Cf=1 pF)	High	Low

Low: 0 V (GND), High: 5 V(Vdd)

Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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