

CMOS linear image sensor



S11108

Achieves high sensitivity by adding an amplifier to each pixel

The S11108 is a CMOS linear image sensor that achieves high sensitivity by adding an amplifier to each pixel. It has a long photosensitive area (effective photosensitive area length: 28.672 mm) consisting of 2048 pixels, each with a pixel size of $14 \times 14 \mu m$.

Features

- → Pixel size: 14 × 14 µm
- 2048 pixels
- Effective photosensitive area length: 28.672 mm
- → High sensitivity: 50 V/(lx·s)
- ➡ Simultaneous charge integration for all pixels
- **→** Variable integration time function (electronic shutter function)
- **■** 5 V single power supply operation
- Built-in timing generator allows operation with only start and clock pulse inputs
- Video data rate: 10 MHz max.
- Small input terminal capacitance: 5 pF

- Applications

- → Position detection
- **■** Image reading
- → Encoder
- **■** Barcode reader

Structure

Parameter	Specification	Unit
Number of pixels	2048	-
Pixel size	14 × 14	μm
Photosensitive area length	28.672	mm
Package	LCP (liquid crystal polymer)	-
Window material	Tempax	-

- Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Block switch voltage	V(BSW)	Ta=25 °C	-0.3 to +6	V
Operating temperature	Topr	No condensation*1	-40 to +85	°C
Storage temperature	Tstg	No condensation*1	-40 to +85	°C

^{*1:} When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

➡ Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Тур.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
Clock pulse voltage	Low level	V(CLK)	0	-	0.3	V
Start pulse voltage	High level	\//CT\	3	Vdd	Vdd + 0.25	V
Start pulse voltage	Low level	V(ST)	0	-	0.3	V
Block switch voltage*2	2048 pixels reading	V(BSW)	0	-	0.3	V
block Switch voltage -	1024 pixels reading	v(DSW)	3	Vdd	Vdd + 0.25	V

^{*2:} This should be NC or GND when reading from all pixels, or Vdd when reading from 1024 pixels (513 to 1536 channels).

■ Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

■ Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Тур.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	-	10 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption*3 *4	Ic	20	30	50	mA

^{*3:} f(CLK)=10 MHz

■ Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

Parameter	Symbol	Min.	Тур.	Max.	Unit
Spectral response range	λ		400 to 1000		nm
Peak sensitivity wavelength	λр	-	700	-	nm
Photosensitivity*5	S	-	50	-	V/(lx·s)
Conversion efficiency*6	CE	-	13	-	μV/e-
Dark output voltage*7	Vd	0	0.3	3	mV
Saturation output voltage*8	Vsat	0.9	1.2	1.7	V
Readout noise	Nread	0.3	0.6	1.5	mV rms
Dynamic range 1*9	Drange1	-	2000	-	times
Dynamic range 2*10	Drange2	-	4000	-	times
Output offset voltage	Voffset	0.4	0.5	0.8	V
Photoresponse nonuniformity*5 *11	PRNU	-	±2	±10	%
Image lag *12	IL	-	-	0.6	mV

^{*5:} Measured with a tungsten lamp of 2856 K

Integration time Ts=10 ms

Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.

*11: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 2042 pixels excluding 3 pixels each at both ends, and is defined as follows:

PRNU= $\Delta X / X \times 100$ (%)

X: average output of all pixels, ΔX : difference between X and maximum output or minimum output

*12: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state



^{*4:} Current consumption increases as the clock pulse frequency increases. The current consumption is 10 mA typ. at f(CLK)=200 kHz.

^{*6:} Output voltage generated per one electron

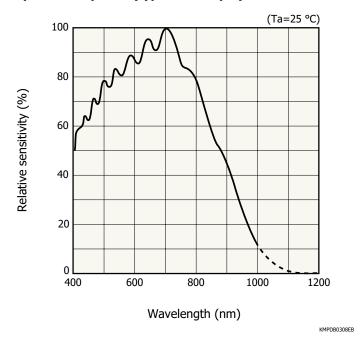
^{*7:} Integration time Ts=10 ms

^{*8:} Difference from Voffset

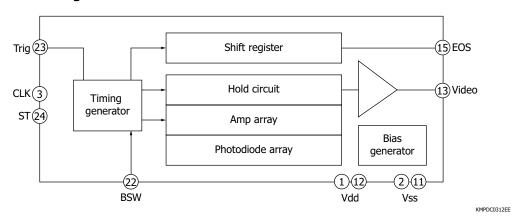
^{*9:} Drange1= Vsat/Nread

^{*10:} Drange2= Vsat/Vd

Spectral response (typical example)

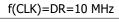


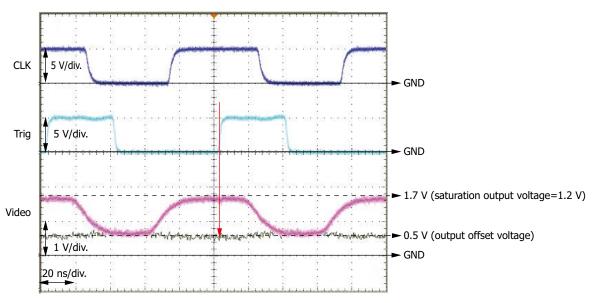
Block diagram



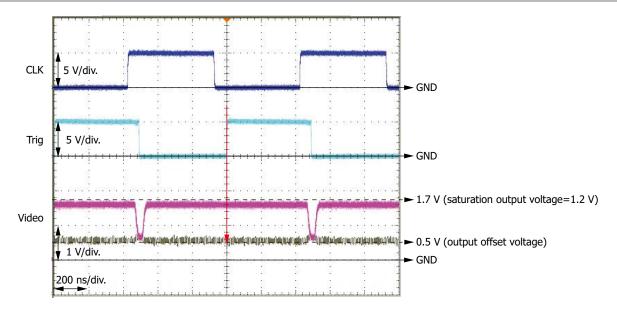
Output waveform of one pixel

The timing for acquiring the Video signal is synchronized with the rising edge of a trigger pulse (See red arrow below.).

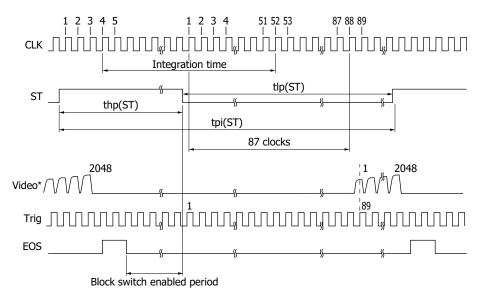




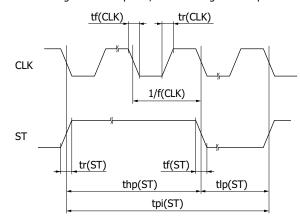
f(CLK)=DR=1 MHz



- Timing chart



* When reading from 1024 pixels, the Video signal is output from 513 to 1536 channels.



KMPDC0319EF

Parameter	Symbol	Min.	Тур.	Max.	Unit
Start pulse cycle*13	tpi(ST)	98/f(CLK)	-	-	S
Start pulse high period*13 *14	thp(ST)	6/f(CLK)	-	-	S
Start pulse low period	tlp(ST)	92/f(CLK)	-	-	S
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

^{*13:} Dark output increases if the start pulse cycle or the start pulse high period is lengthened.

The shift register starts operation at the rising edge of CLK immediately after ST goes low.

The integration time can be changed by changing the ratio of the high and low periods of ST.

If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.



^{*14:} The integration time equals the high period of ST plus 48 CLK cycles.

- Operation example

For outputting signals from all 2048 channels

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 2048 channels)

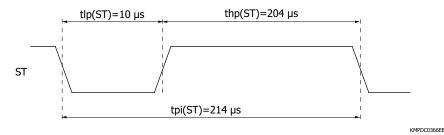
Clock pulse frequency = Video data rate = 10 MHz

Start pulse cycle = 2140/f(CLK) = 2140/10 MHz = 214 μ s

High period of start pulse = Start pulse cycle - Start pulse's low period min.

= $2140/f(CLK) - 92/f(CLK) = 2140/10 \text{ MHz} - 92/10 \text{ MHz} = 204.8 \ \mu s$

Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be 204.8 + 4.8 = 209.6 µs.



For outputting signals from 1024 channels (513 to 1536 channels)

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized [for outputting signals from 1024 channels (513 to 1536 channels)]

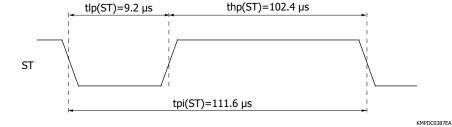
Clock pulse frequency = Video data rate = 10 MHz

Start pulse cycle = $1116/f(CLK) = 1116/10 \text{ MHz} = 111.6 \mu s$

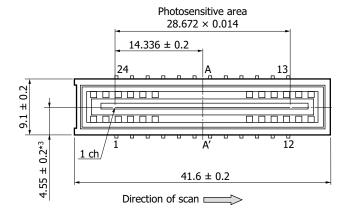
High period of start pulse = Start pulse cycle - Start pulse's low period min.

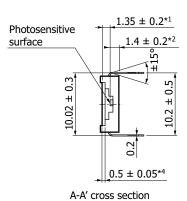
= $1116/f(CLK) - 92/f(CLK) = 1116/10 \text{ MHz} - 92/10 \text{ MHz} = 102.4 \mu s$

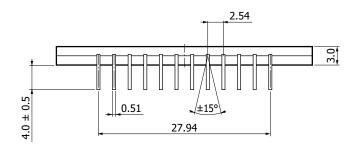
Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be $102.4 + 4.8 = 107.2 \mu s$.



Dimensional outline (unit: mm)







Tolerance unless otherwise noted: ±0.1

- *1: Distance from window upper
- surface to photosensitive surface *2: Distance from package bottom to photosensitive surface
- *3: Distance from package edge to photosensitive area center *3: Glass thickness

KMPDA0250EH

- Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	13	Video	0	Video signal
2	Vss	-	GND	14	NC	-	No connection
3	CLK	I	Clock pulse	15	EOS	0	End of scan
4	NC	-	No connection	16	NC	-	No connection
5	NC	-	No connection	17	NC	-	No connection
6	NC	-	No connection	18	NC	-	No connection
7	NC	-	No connection	19	NC	-	No connection
8	NC	-	No connection	20	NC	-	No connection
9	NC	-	No connection	21	NC	-	No connection
10	NC	-	No connection	22	BSW	-	Block switch*15
11	Vss	-	GND	23	Trig	0	Trigger pulse for video signal acquisition
12	Vdd	I	Supply voltage	24	ST	I	Start pulse

Note: Leave the "NC" terminals open and do not connect them to GND.

Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance operational amplifier with JFET or CMOS input.

*15: This should be NC or GND when reading from all pixels, or Vdd when reading from 1024 pixels (513 to 1536 channels).

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (5 seconds or less)	

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

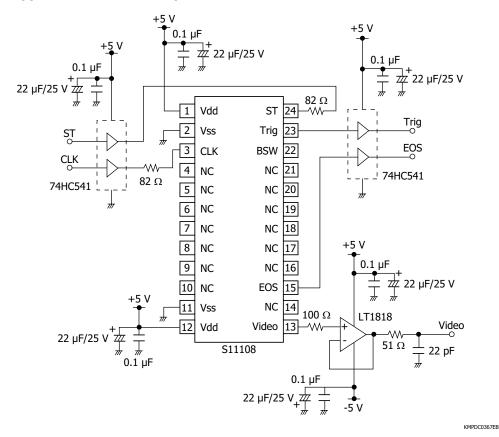
(2) Light input window

If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) UV exposure

This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.

Application circuit example



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S11108

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

- Precautions
- Disclaimer
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- Technical note
- · CMOS linear image sensors

Information described in this material is current as of March 2024.

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