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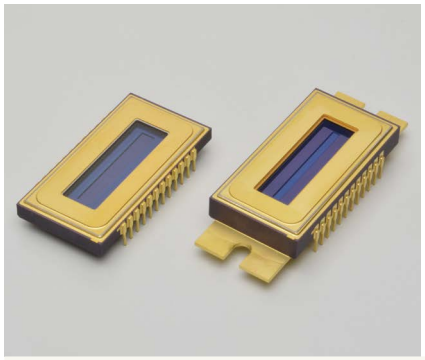
CCD area image sensors



S12600/S12601 series

Back-thinned FFT-CCD

The S12600/S12601 series are measurement type FFT-CCD area image sensors developed for low-light-level detection. By using the binning operation, they can be used as a linear image sensor having a long side aligned along the height direction of the photosensitive area. This makes them suited for use in spectrophotometry detectors. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S12600/S12601 series are now capable of high-speed readout due to the reduced resistance in the register wiring and the adoption of a high-speed amplifier.

Features

- **One-stage TE-cooled type (S12601 series)**
- **Pixel size: 24 × 24 µm**
- **Line/pixel binning capabilities**
- **Quantum efficiency: 90% or higher at peak**
- **Wide spectral response range**
- **High-speed readout (fc=5 MHz max.)**
- **Wide dynamic range**
- **MPP operation**
- **High UV sensitivity and stable characteristics under UV light irradiation**
- **Fill factor: 100%**

Applications

- **Fluorescence spectrophotometry, ICP**
- **Industrial product inspection**
- **Semiconductor inspection**
- **DNA sequencer**
- **Low-light-level detection**

Selection guide

Type no.	Cooling	Total number of pixels	Number of effective pixels	Image size [mm (H) × mm (V)]
S12600-1006	Non-cooled	1044 × 64	1024 × 58	24.576 × 1.392
S12600-1007		1044 × 128	1024 × 122	24.576 × 2.928
S12601-1006S	One-stage TE-cooled	1044 × 64	1024 × 58	24.576 × 1.392
S12601-1007S		1044 × 128	1024 × 122	24.576 × 2.928

Structure

Parameter	S12600 series	S12601 series
Pixel size (H × V)	24 × 24 µm	
Vertical clock	2-phase	
Horizontal clock	2-phase	
Output circuit	Two-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outlines)	
Window material*1	Quartz glass*2	AR-coated sapphire*3

*1: Temporary window type (S12600-1006N/-1007N) is also available upon request.
*2: Resin sealing
*3: Hermetic sealing

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature*4 *5	Topr		-50	-	+50	°C
Storage temperature*5	Tstg		-50	-	+70	°C
Output transistor drain voltage	VOD		-0.5	-	+20	V
Reset drain voltage	VRD		-0.5	-	+18	V
Output amplifier feedback voltage	Vret		-0.5	-	+18	V
Vertical input source voltage	VISV		-0.5	-	+18	V
Horizontal input source voltage	VISH		-0.5	-	+18	V
Vertical input gate voltage	VIG1V, VIG2V		-10	-	+15	V
Horizontal input gate voltage	VIG1H, VIG2H		-10	-	+15	V
Summing gate voltage	VSG		-10	-	+15	V
Output gate voltage	VOG		-10	-	+15	V
Reset gate voltage	VRG		-10	-	+15	V
Transfer gate voltage	VTG		-10	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V		-10	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H		-10	-	+15	V
Maximum current of TE-cooler*6	Imax	Tc*7=Th*8=25 °C	-	-	3.0	A
Maximum voltage of TE-cooler	Vmax	Tc*7=Th*8=25 °C	-	-	3.6	V
Maximum temperature of the heat radiation side of the TE-cooler	-		-	-	70	°C

*4: Package temperature (S12600 series), chip temperature (S12601 series)
*5: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*6: When the current value exceeds Imax, the heat absorption rate begins to decrease due to the Joule heat. This maximum current Imax is not the threshold for damaging the TE-cooler. To protect the TE-cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*7: Temperature of the cooling side of the TE-cooler
*8: Temperature of the heat radiation side of the TE-cooler
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			VOD	14	15	16	V
Reset drain voltage			VRD	13	14	15	V
Output amplifier feedback voltage*9			Vret	1.5	2	3	V
Output gate voltage			VOG	1	3	5	V
Substrate voltage			VSS	-	0	-	V
Test point	Vertical input source		VISV	-	VRD	-	V
	Horizontal input source		VISH	-	VRD	-	V
	Vertical input gate		VIG1V, VIG2V	-9	-8	-	V
	Horizontal input gate		VIG1H, VIG2H	-9	-8	-	V
Vertical shift register clock voltage		High	VP1VH, VP2VH	4	6	8	V
		Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage		High	VP1HH, VP2HH	4	6	8	V
		Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage		High	VSGH	4	6	8	V
		Low	VSGL	-9	-8	-7	
Reset gate voltage		High	VRGH	5	7	9	V
		Low	VRGL	-9	-8	-7	
Transfer gate voltage		High	VTGH	4	6	8	V
		Low	VTGL	-9	-8	-7	
External load resistance			RL	1	2.2	3	kΩ

*9: The output amplifier feedback voltage is positive relative to the substrate voltage, but the current flows from the sensor.

Electrical characteristics [Ta=25 °C, fc=3 MHz, operating conditions: Typ. (P.2), timing chart (P.6)]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	0.1	3	5	MHz
Vertical shift register capacitance	S12600-1006, S12601-1006S	C_{P1V}, C_{P2V}	-	1500	-	pF
	S12600-1007, S12601-1007S		-	3000	-	
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	180	-	pF
Summing gate capacitance		C_{SG}	-	30	-	pF
Reset gate capacitance		C_{RG}	-	15	-	pF
Transfer gate capacitance		C_{TG}	-	75	-	pF
Charge transfer efficiency*10		CTE	0.99995	0.99999	-	-
DC output level*11		Vout	9	10	11	V
Output impedance*11		Zo	-	200	-	Ω
Power consumption*11 *12		P	-	90	100	mW

*10: Charge transfer efficiency per pixel, measured at half of the saturation output
*11: Varies depending on the load resistance. (Typ. V_{OD}=15 V, load resistance=2.2 kΩ)
*12: Power consumption of the on-chip amp plus load resistance

Electrical and optical characteristics [Ta=25 °C, fc=3 MHz, operating conditions: Typ. (P.2), timing chart (P.6)]

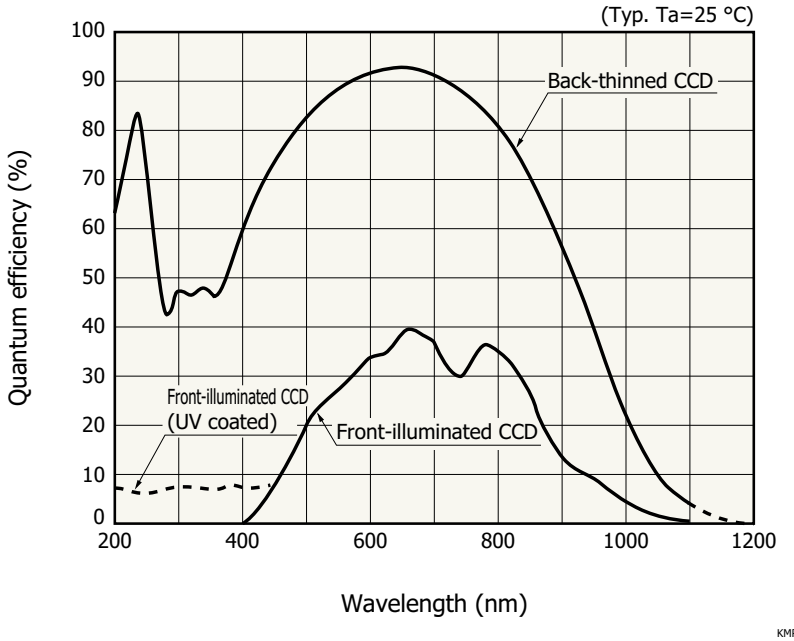
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Saturation charge	Vertical		Fw	240	320	-	ke^-
	Horizontal*13			800	1000	-	
Conversion efficiency			CE	1.8	2.2	3	$\mu V/e^-$
Dark current*14 (MPP mode)	25 °C		DS	-	100	1000	e^-/pixel/s
	0 °C			-	10	100	
Readout noise*15			Nread	20	30	40	e^- rms
Dynamic range*16	Line binning		Drange	20000	33000	-	-
	Area scanning			6000	10700	-	-
Photoresponse nonuniformity*17			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*18	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect*19			-	-	3	-
	Column defect*20			-	-	0	-

*13: Linearity=±1.5%
*14: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*15: Using a Hamamatsu evaluation circuit (with CDS circuit, chip temperature: 0 °C, operating frequency: 3 MHz)
*16: Dynamic range=Saturation charge/Readout noise
*17: Measured at one-half of the saturation output using LED light (peak emission wavelength: 560 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

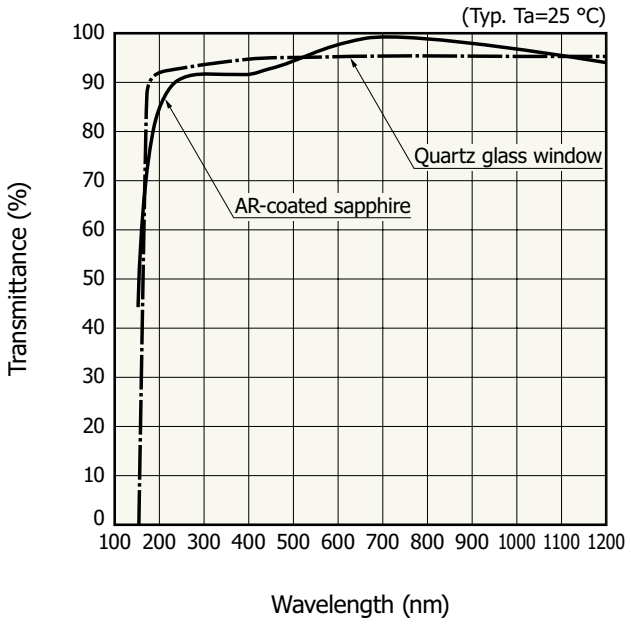
*18: White spots
Pixels whose dark current is higher than 1 ke- after one-second integration at a cooling temperature of 0 °C
Black spots
Pixels whose sensitivity is lower than one half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*19: 2 to 9 consecutive image defects
*20: 10 or more consecutive image defects

Spectral response (without window)*21

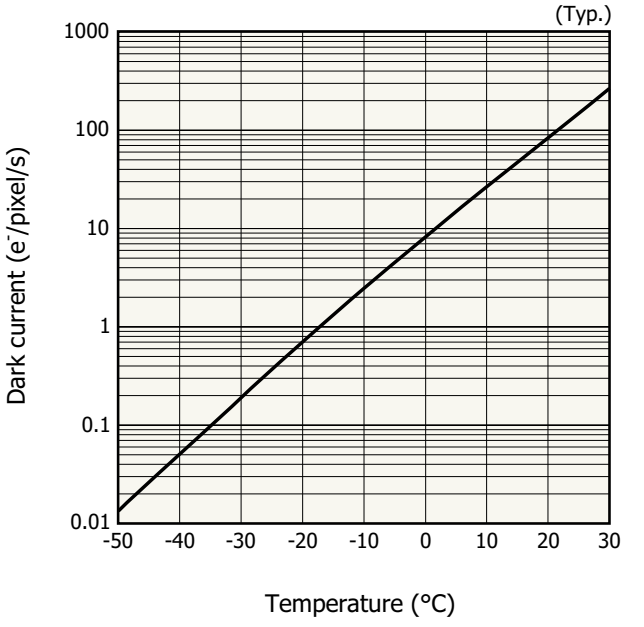


*21: Spectral response is decreased according to the spectral transmittance characteristics of the quartz glass or AR-coated sapphire.

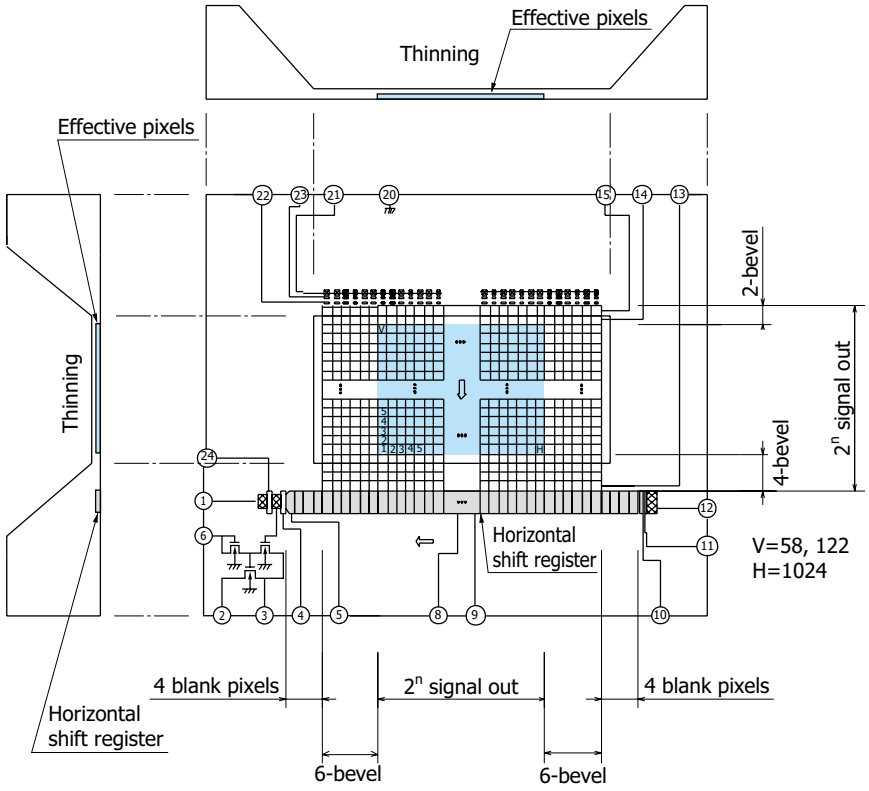
Spectral transmittance characteristics of window material



Dark current vs. temperature



Device structure (schematic of CCD chip as viewed from top of dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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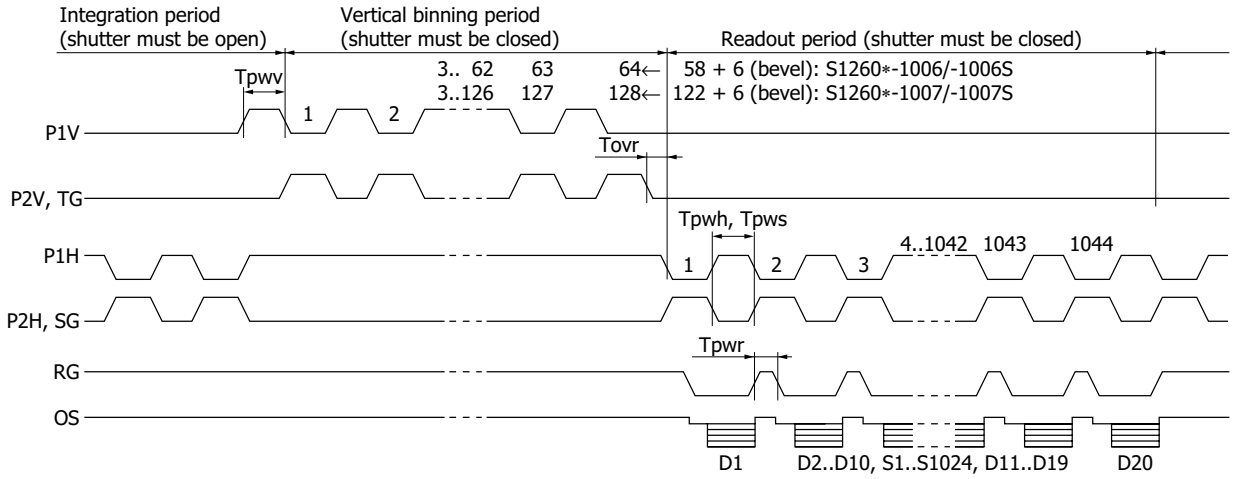
Timing chart

Line binning

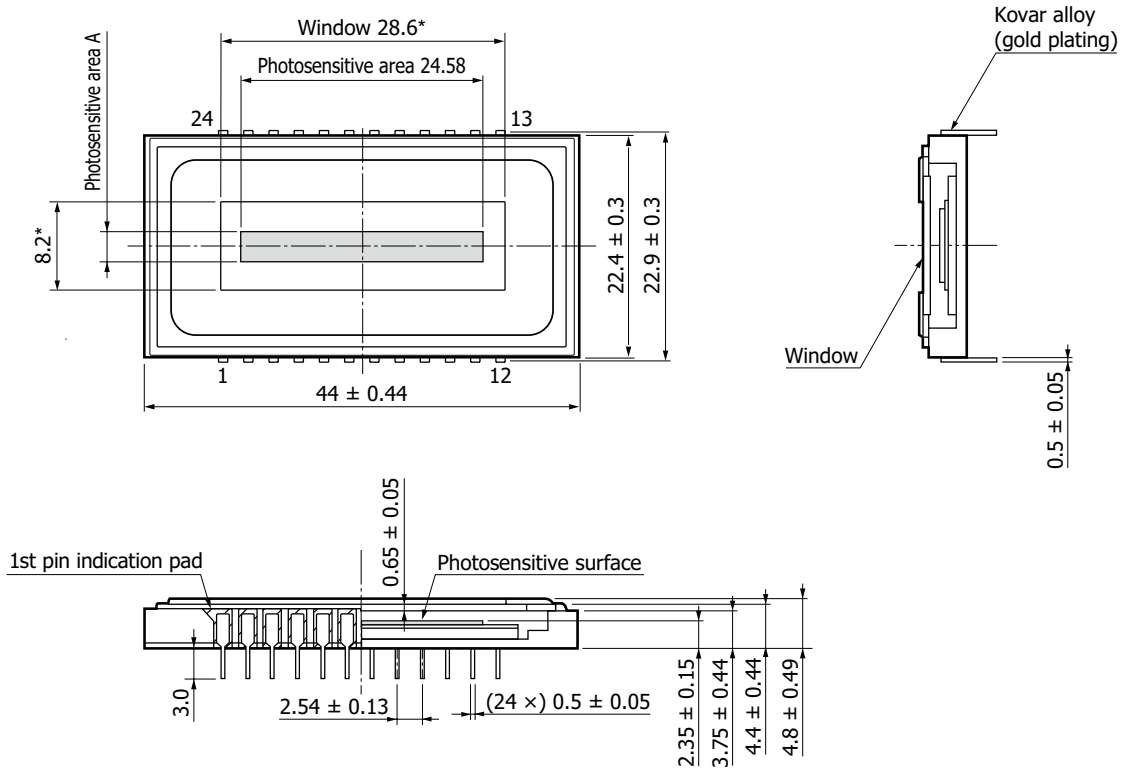


Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*22	Pulse width	S12600-1006, S12601-1006S	Tpwv	0.5	1	-	µs
		S12600-1007, S12601-1007S		1	2	-	
	Rise and fall times		Tprv, Tpfv	20	-	-	ns
P1H, P2H*21	Pulse width		Tpwh	100	166	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	100	166	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	20	33	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG – P1H	Overlap time		Tovr	1	2	-	µs

*22: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outlines (unit: mm)

S12600 series



S12600-1006: A=1.392
S12600-1007: A=2.928

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph
Weight: 11.9 g

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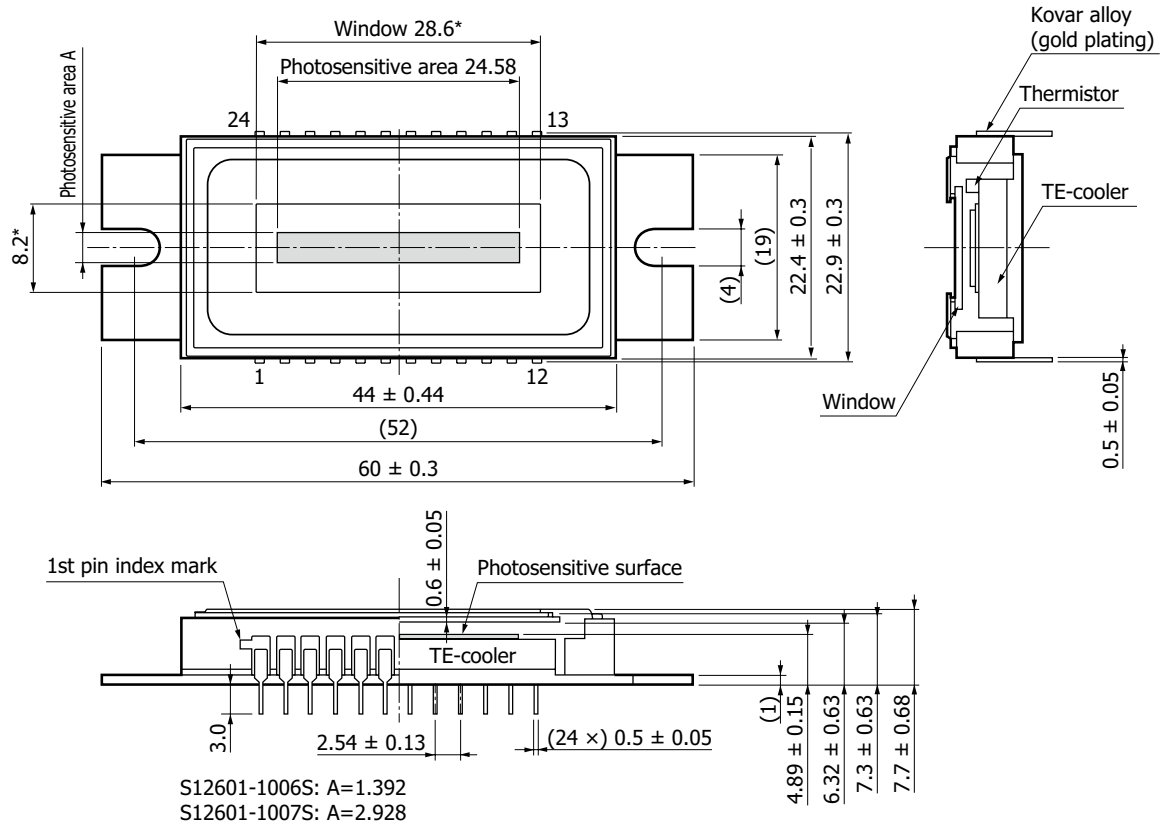
S12601 series



S12601-1006S: A=1.392
S12601-1007S: A=2.928

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph
Weight: 38.7 g

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Pin connections

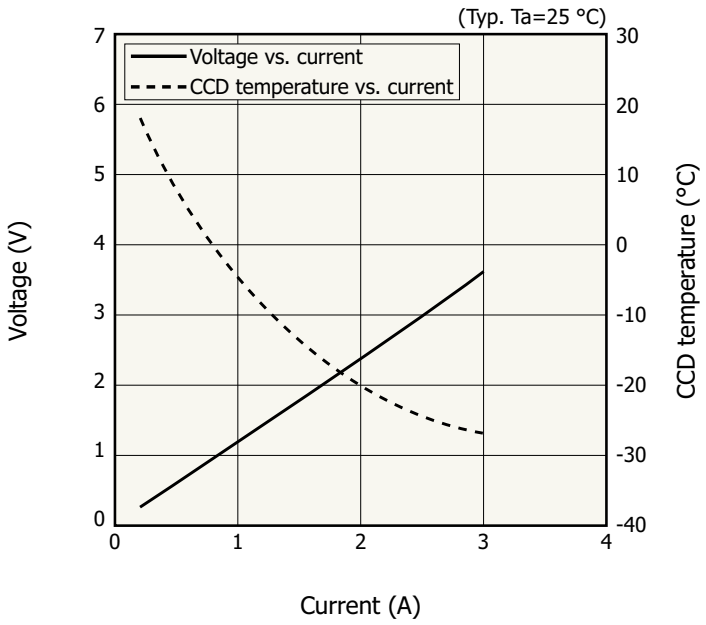
Pin no.	S12600 series		S12601 series		Note
	Symbol	Function	Symbol	Function	(standard operation)
1	RD	Reset drain	RD	Reset drain	+14 V
2	OS	Output transistor source	OS	Output transistor source	RL=2.2 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+15 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same timing as P2H
6	Vret	Output amplifier feedback voltage	Vret	Output amplifier feedback voltage	+2 V
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*23	Transfer gate	TG*23	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler (-)	
19	-		P+	TE-cooler (+)	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

*23: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	1.2	Ω
Maximum heat absorption*24	Qmax		5.1	W

*24: This is a theoretical heat absorption level for correcting the temperature difference that occurs in the TE-cooler when the maximum current is supplied.



The temperature of the heat radiation side must be set to 30 °C or lower to make the cooling area -10 °C. As a guideline, use a heatsink whose thermal resistance is 1°C/W or lower.

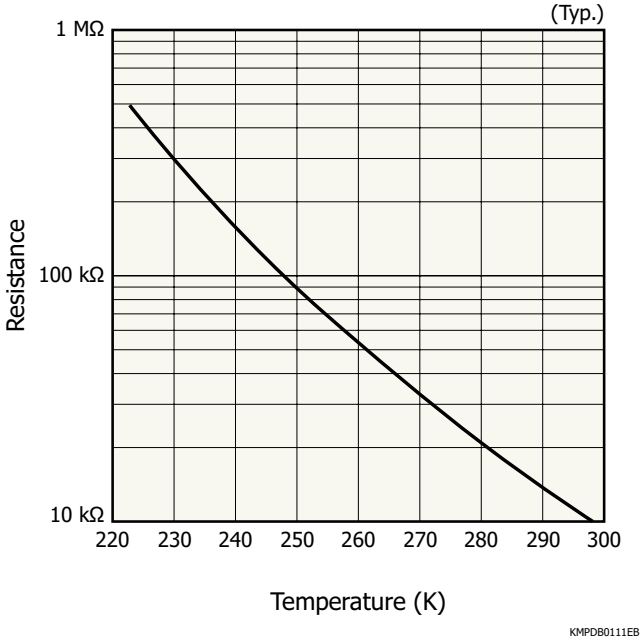
Specifications of built-in temperature sensor

A thermistor chip is built into the same package with a CCD chip and monitors the operating CCD chip temperature.
The relation between this thermistor's resistance and absolute temperature is express by the following equation.

$$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$$

R_{T1}: resistance at absolute temperature T1 [K]
R_{T2}: resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place the sensor directly on workbenches or floors that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Temperature gradient rate for cooling or heating of element

When using an external cooler, set the temperature gradient rate for cooling or heating the element to 5 K/minute or less.

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (once, within 5 seconds)	At least 2 mm away from lead roots

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical note
· CCD image sensor

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