CMOS linear image sensor

S12706

High sensitivity, photosensitive area with minute pixels

The S12706 is a high sensitivity CMOS linear image sensor using a photosensitive area with minute pixels. It has a long photosensitive area (effective photosensitive length: 28.672 mm) consisting of 4096 pixels, each with a pixel size of 7 × 7 µm.

Features

- **Pixel size: 7 × 7 µm**
- **4096 pixels**
- **Effective photosensitive area length: 28.672 mm**
- **High sensitivity: 23 V/($lx·s$)**
- **Simultaneous charge integration for all pixels**
- **Variable integration time function (electronic shutter function)**
- **5 V single power supply operation**
- **Built-in timing generator allows operation with only start and clock pulse inputs.**
- **Video data rate: 10 MHz max.**

Applications

- **Position detection**
- **Image reading**
- **Encoders**

Structure

Parameter	Specification	Unit
Number of pixels	4096	-
Pixel size	7 × 7	µm
Photosensitive area length	28.672	mm
Package	LCP (liquid crystal polymer)	-
Window material	Borosilicate glass	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Operating temperature[1]	Topr		-40 to +85	°C
Storage temperature[1]	Tstg		-40 to +85	°C

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

[1]: No condensation

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V
Start pulse voltage	High level	V(ST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V

Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	5 M	10 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption[*2][*3]	Ic	20	40	60	mA

*2: f(CLK)=10 MHz
*3: Current consumption increases as the clock pulse frequency increases. The current consumption is 10 mA typ. at f(CLK)=200 kHz.

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		400 to 1000		nm
Peak sensitivity wavelength	λp	-	600	-	nm
Photosensitivity[*4]	S	-	23	-	V/($lx\cdot$s)
Conversion efficiency[*5]	CE	-	25	-	μV/e⁻
Dark output voltage[*6]	Vd	0	0.2	2	mV
Saturation output voltage[*7][*8]	Vsat	1.5	2.0	2.5	V
Readout noise	Nread	0.5	1.0	1.8	mV rms
Dynamic range 1[*9]	Drange1	-	2000	-	times
Dynamic range 2[*10]	Drange2	-	10000	-	times
Output offset voltage	Voffset	0.3	0.5	0.9	V
Photoresponse nonuniformity[*4][*11]	PRNU	-	±2	±10	%
Image lag[*12]	IL	-	-	0.1	%

*4: Measured with a tungsten lamp of 2856 K
*5: Output voltage generated per one electron
*6: Integration time=10 ms
*7: Diference from Voffset
*8: CDS (correlated double sampling) is done inside the image sensor in order to reduce noise. The final output is the difference between the output when the photosensitive area is put in the reset state, and the light output integrated in the photosensitive area. If used in an over-saturated state, the light output component may get mixed into the output when the photosensitive area is put in the reset state, causing the final output to decrease.
*9: Drange1 = Vsat/Nread
*10: Drange2 = Vsat/Vd
   Integration time=10 ms
   Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.
*11: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 4090 pixels excluding 3 pixels each at both ends, and is defined as follows:
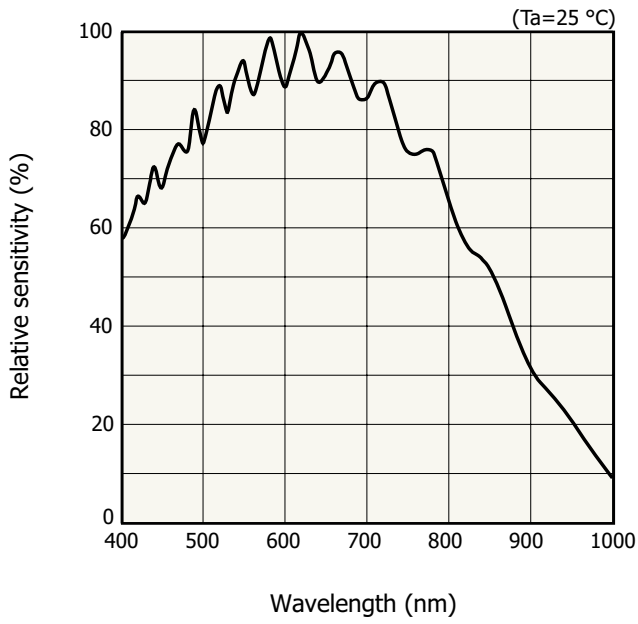   PRNU = ΔX/X × 100 (%)
   X: average output of all pixels, ΔX: difference between X and maximum output or minimum output
*12: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state.
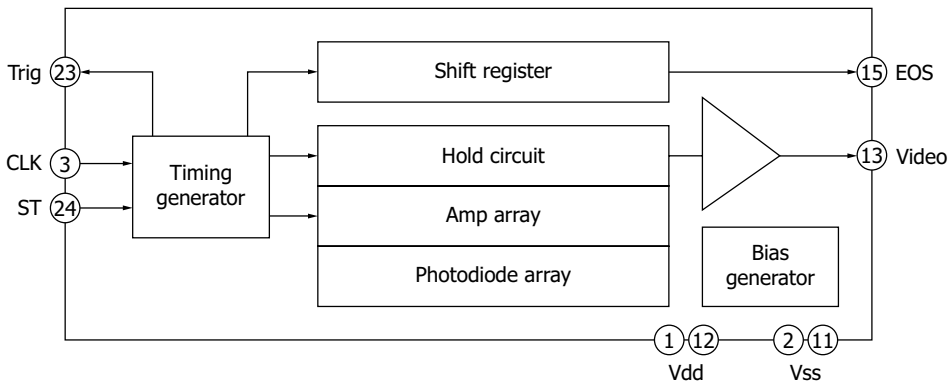   Image lag increases when the output exceeds the saturation output voltage.
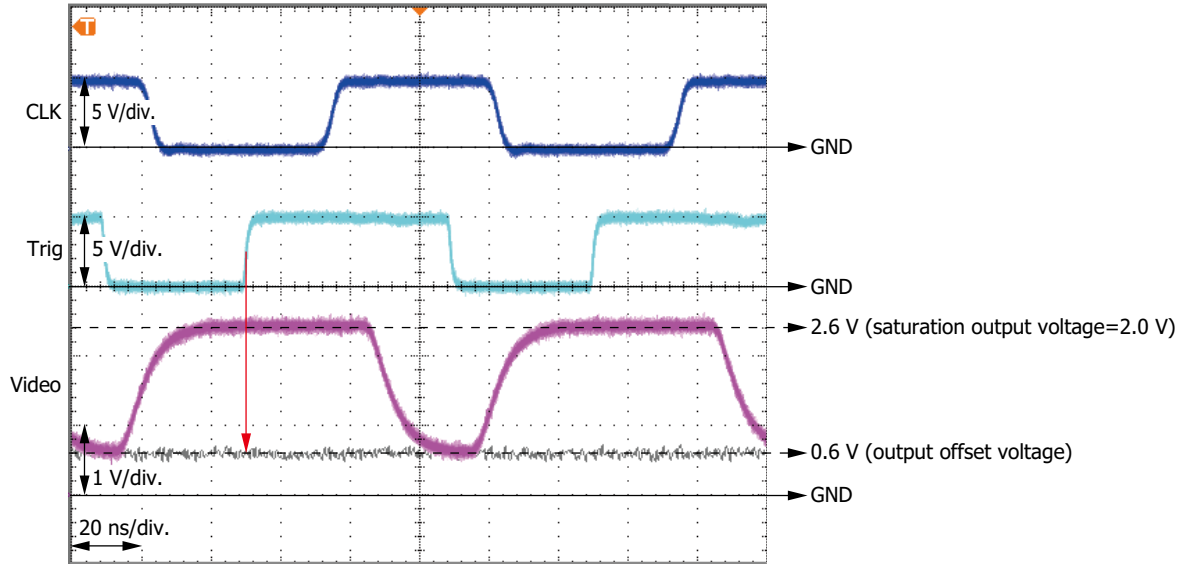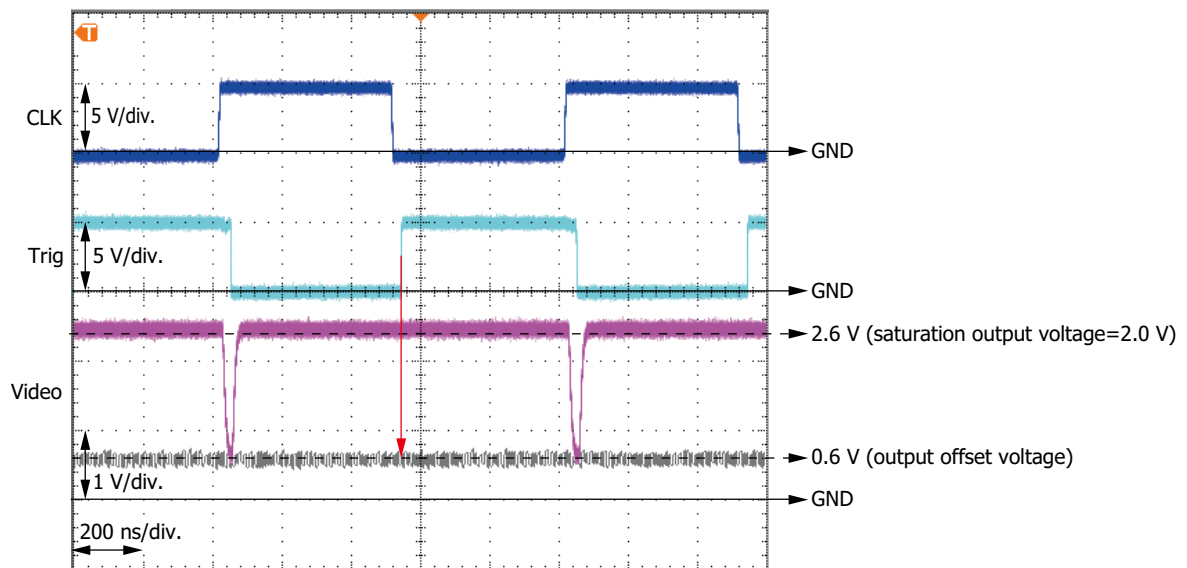
Spectral response (typical example)

Relative sensitivity (%) vs Wavelength (nm)

(Ta=25 °C)

KMPDB0397EA

Block diagram

Trig (23)

CLK (3)

ST (24)

Timing generator

Shift register → (15) EOS

Hold circuit

Amp array

Photodiode array

Bias generator

Video (13)

(1)(12) Vdd   (2)(11) Vss

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Output waveforms of one pixel

The timing for acquiring the Video signal is synchronized with the rising edge of Trig pulse (See red arrow below.).

f(CLK)=DR=10 MHz

CLK   5 V/div.   GND
Trig   5 V/div.   GND
                                    2.6 V (saturation output voltage=2.0 V)
Video
                                    0.6 V (output offset voltage)
        1 V/div.   GND
        20 ns/div.

f(CLK)=DR=1 MHz

CLK   5 V/div.   GND
Trig   5 V/div.   GND
                                    2.6 V (saturation output voltage=2.0 V)
Video
                                    0.6 V (output offset voltage)
        1 V/div.   GND
        200 ns/div.

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Timing chart
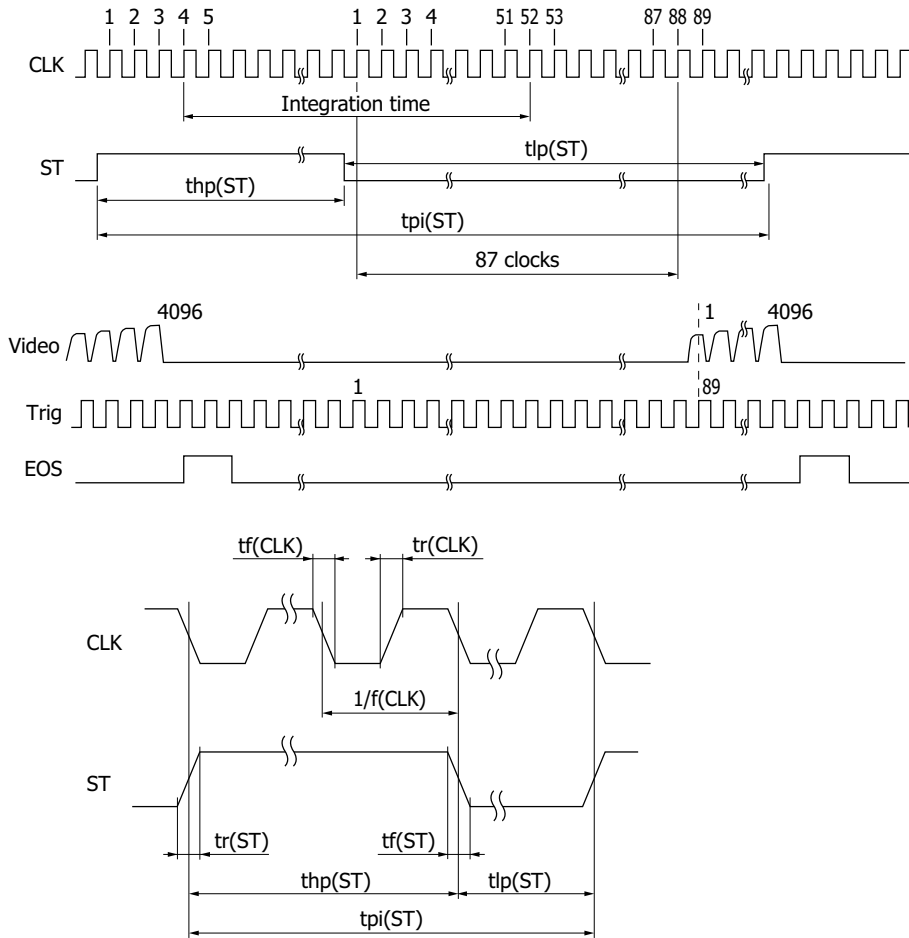
KMPDC0480EA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse cycle[13]	tpi(ST)	98/f(CLK)	-	-	s
Start pulse high period[13] [14]	thp(ST)	6/f(CLK)	-	-	s
Start pulse low period	tlp(ST)	92/f(CLK)	-	-	s
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty ratio	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

[13]: Dark output increases if the start pulse cycle or the start pulse high period is lengthened.
[14]: The integration time equals the high period of ST plus 48 CLK cycles.
The shift register starts operation at the rising edge of CLK immediately after ST goes low.
The integration time can be changed by changing the ratio of the high and low periods of ST.
If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.

Operation example

■ When outputting from all 4096 pixels

This example assumes that the clock pulse frequency is maximized (data rate is also maximized), the time of one scan is minimized, and the integration time is maximized

Clock pulse frequency = Data rate = 10 MHz

Start pulse cycle = 4188/f(CLK) = 4188/10 MHz = 418.8 µs

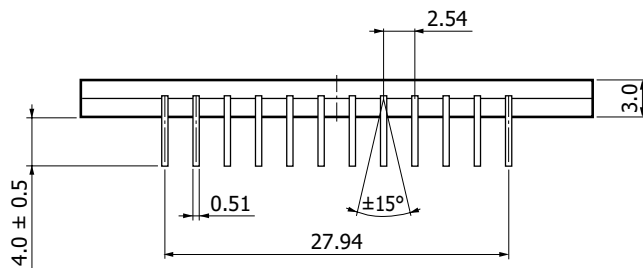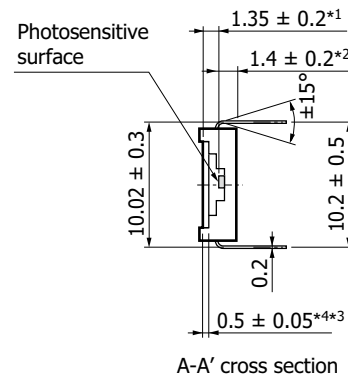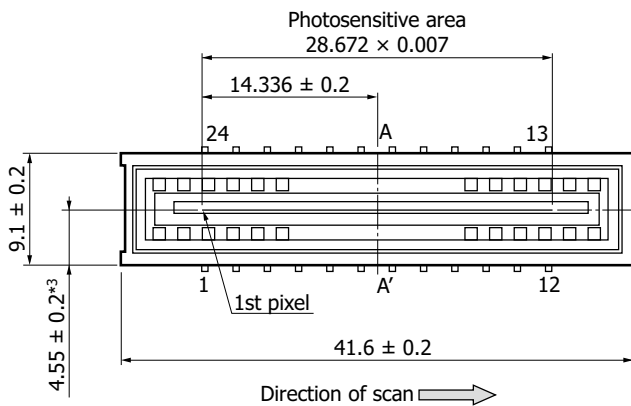High period of start pulse = Start pulse cycle - Start pulse's low period min.

= 4188/f(CLK) - 92/f(CLK) = 4188/10 MHz - 92/10 MHz = 409.6 µs

Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be 409.6 + 4.8 = 414.4 µs.
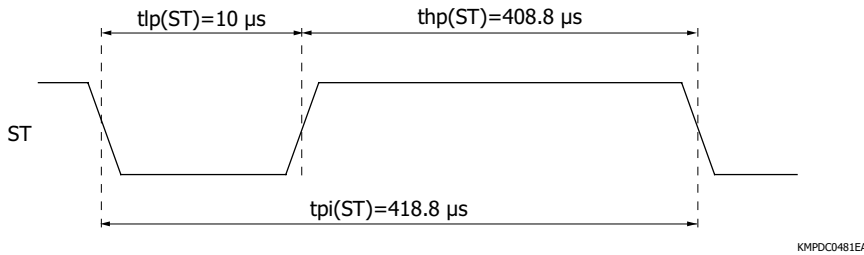
KMPDC0481EA

Dimensional outline (unit: mm)

Tolerance unless otherwise noted: ±0.1
*1: Distance from window upper surface to photosensitive surface
*2: Distance from package bottom to photosensitive surface
*3: Distance from package edge to photosensitive area center
*4: Glass thickness

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Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	13	Video	O	Video signal*15
2	Vss	-	GND	14	NC	-	No connection
3	CLK	I	Clock pulse	15	EOS	O	End of scan
4	NC	-	No connection	16	NC	-	No connection
5	NC	-	No connection	17	NC	-	No connection
6	NC	-	No connection	18	NC	-	No connection
7	NC	-	No connection	19	NC	-	No connection
8	NC	-	No connection	20	NC	-	No connection
9	NC	-	No connection	21	NC	-	No connection
10	NC	-	No connection	22	NC	-	No connection
11	Vss	-	GND	23	Trig	O	Trigger pulse for video signal acqusition*16
12	Vdd	I	Supply voltage	24	ST	I	Start pulse

*15: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance op-amp with JFET or CMOS input.

*16: We recommend capturing video signal using the trigger pulse output from Trig.

Note: Leave the "NC" terminals open and do not connect them to GND.

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (5 seconds or less)	

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window

If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) UV light irradiation

This device is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.

Application circuit example
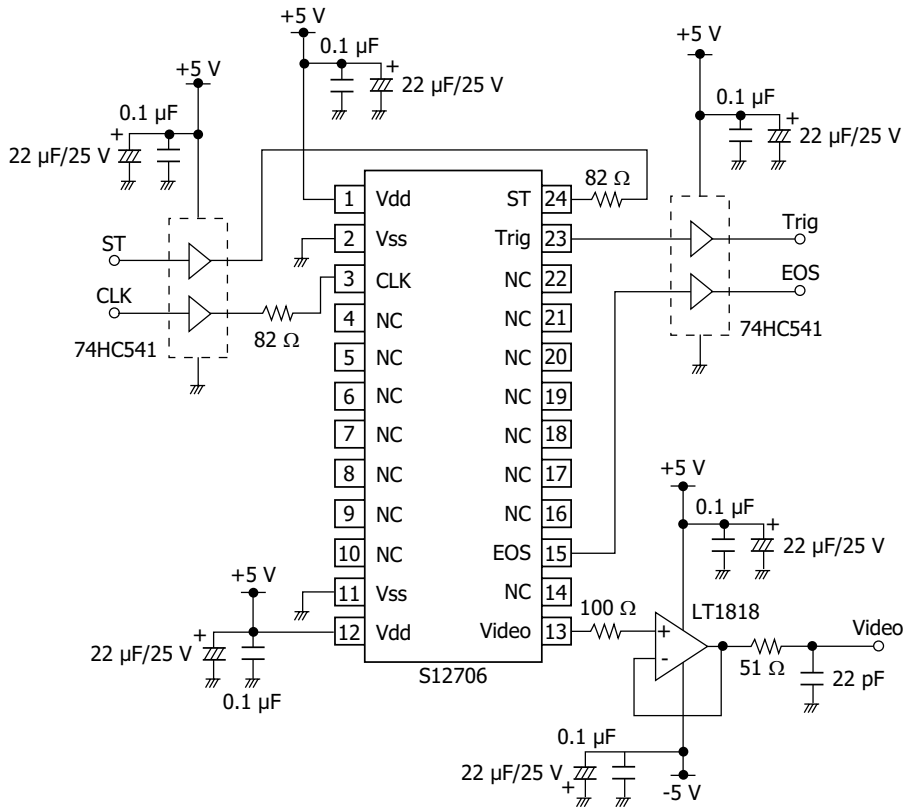
KMPDC0482EA

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors

■ Technical information
· CMOS linear image sensors

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Driver circuit for CMOS linear image sensors C16605 [sold separately]

The driver circuit for CMOS linear image sensor S12706 is available (sold separately).
It can be used for spectrometers, etc. combining with the CMOS linear image sensor.
Contact us for detailed information.

Features

→ **Built-in 16-bit A/D converter**
→ **Interface to computer: USB 2.0**
→ **Power supply: USB bus power operation**

Information described in this material is current as of April 2024.

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