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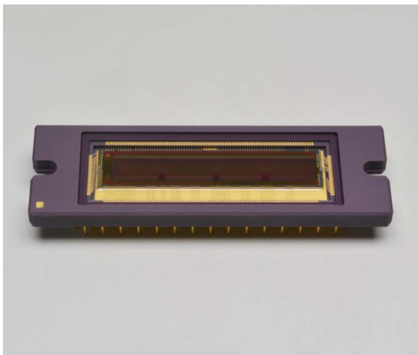


CMOS linear image sensor

S14772

High-speed readout (125 klines/s)

The S14772 is a CMOS linear image sensor developed for industrial cameras that require high-speed scanning. The column-parallel readout system, which has a readout amplifier and an A/D converter for each pixel, allows high-speed readout. For the A/D converter resolution, either 10-bit (high-speed mode: 125 klines/s max.) or 11-bit (low-speed mode: 62.5 klines/s max.) can be selected. Video signal is output serially in 225 MHz LVDS format.

Features

- **Pixel size: 14 × 14 μm**
- **Number of pixels: 2048**
- **High-speed readout: 125 klines/s**
- **Simultaneous integration of all pixels**
- **3.3 V power supply operation**
- **SPI communication function**
- **Built-in 10-bit/11-bit A/D converters**

Applications

- **Machine vision**
- **Film inspection**
- **Printed circuit board appearance inspection**
- **Print inspection**

Structure

Parameter	Specification	Unit
Number of pixels	2048	-
Pixel pitch	14	μm
Pixel height	14	μm
Effective photosensitive area length	28.672	mm
Package	Ceramic	-
Window material*1	Borosilicate glass	-

*1: AR coated (1% or less reflectance at 400 to 800 nm) on both sides

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
	Counter terminal	Vdd(C)		-0.3 to +3.9	V
Digital input signal terminal voltage*2		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*3	-5 to +70	°C
Storage temperature		Tstg	No dew condensation*3	-10 to +70	°C

*2: CS, SCLK, MOSI, RSTB, MCLK, MST, All-reset, PLL-reset

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.15	3.3	3.45	V
	Digital terminal	Vdd(D)	3.15	3.3	3.45	
	Counter terminal	Vdd(C)	3.15	3.3	3.45	
Digital input voltage	High level	Vi(H)	3	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.3	

Electrical characteristics

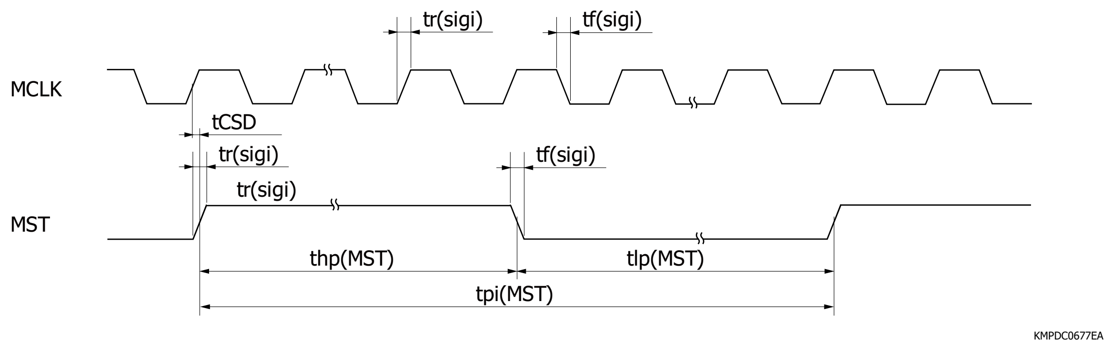
Digital input signal

[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		f(MCLK)	36.5	37.5	38.5	MHz
Master clock pulse duty cycle		D(MCLK)	45	50	55	%
Master start pulse cycle*4	High-speed mode	tpi(MST)	300/f(MCLK)	-	-	s
	Low-speed mode		600/f(MCLK)	-	-	
Master start pulse High period*4	High-speed mode	thp(MST)	166/f(MCLK)	-	-	s
	Low-speed mode		332/f(MCLK)	-	-	
Master start pulse Low period*4	High-speed mode	tlp(MST)	2/f(MCLK)	-	-	s
	Low-speed mode		4/f(MCLK)	-	-	
Master clock - Master start delay time		tCSD	-	-	5	ns
Master clock - Reset delay time*5		tCRD	-	-	5	ns
Rise time*6		tr(sigi)	-	5	7	ns
Fall time*6		tf(sigi)	-	5	7	ns

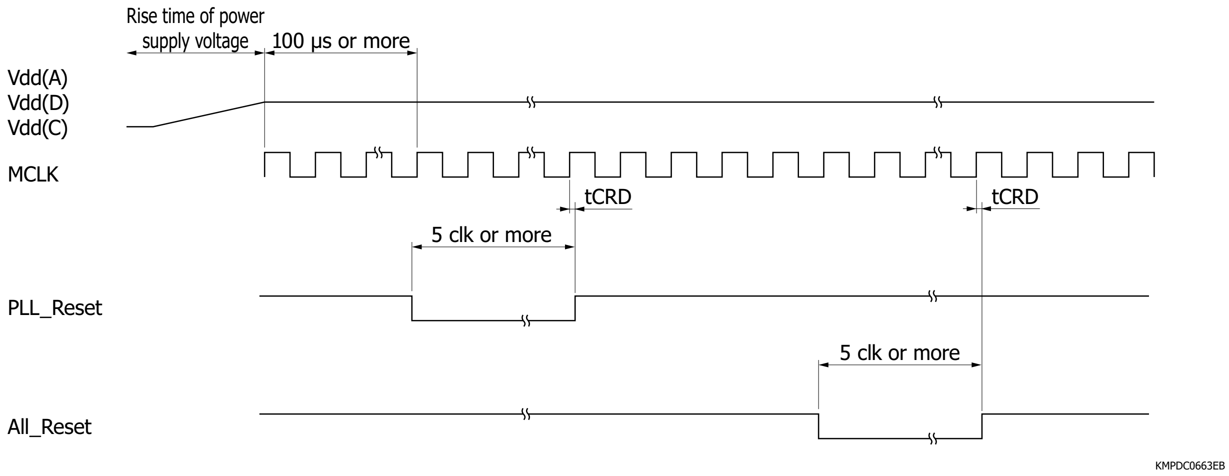
*4: The maximum line rate is 125 klines/s in high-speed mode. Line rate is 125 klines/s when tpi(MST) = 300/f(MCLK).
The maximum line rate is 62.5 klines/s in low-speed mode. Line rate is 62.5 klines/s when tpi(MST) = 600/f(MCLK).
*5: Delay time for the rising edge of MCLK and those of PLL_Reset and All_Reset
*6: Time for the input voltage to rise or fall between 10% and 90%

MCLK and MST input timings



PLL_Reset, All_Reset input timing

After 100 μs of turning on the power, set PLL_Reset to low level for at least 5 master clock cycles and then do the same for All_Reset.



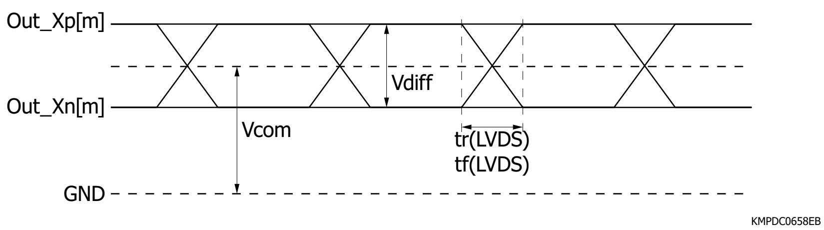
Digital output signal

[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz]

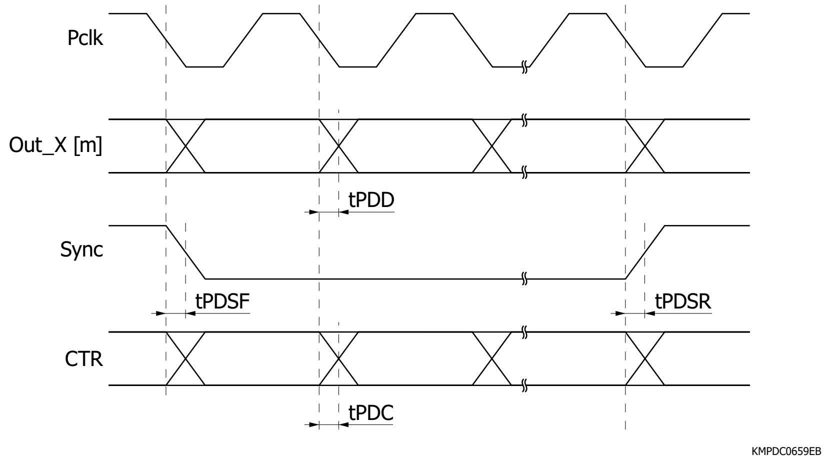
Parameter		Symbol	Min.	Typ.	Max.	Unit
Data rate (LVDS)		DR	f(MCLK)×6			MHz
Line rate	High-speed mode	LR	-	-	125	klines/s
	Low-speed mode		-	-	62.5	
LVDS output voltage*7	Offset	Vcom	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	
LVDS rise time*8		tr(LVDS)	-	0.9	1.3	ns
LVDS fall time*8		tf(LVDS)	-	0.9	1.3	ns
Pclk – OutX[m] delay period		tPDD	-1.0	0.5	2.0	ns
Pclk – CTR delay period		tPDC	-0.5	1.0	2.5	ns
Pclk – Sync delay period	Rise time	tPDSR	-2.5	-1.0	0.5	ns
	Fall time	tPDSF	-2.5	-1.0	0.5	
CMOS output voltage	High	Vsigo(H)	Vdd(D)-0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	
Clock pulse frequency of timing generator	High-speed mode	f(TGCLK)	-	f(MCLK)	-	MHz
	Low-speed mode		-	f(MCLK)/2	-	
CMOS output rise time*9		tr(sigo)	-	10	12	ns
CMOS output fall time*9		tf(sigo)	-	10	12	ns

*7: Attach a 100 Ω terminator to the LVDS output terminal.
*8: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal
*9: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal

LVDS output voltage, rise and fall time



■ Output timing of Sync signal and video output



· Each waveform represents the difference between the LVDS positive signal and negative signal.
· Out_X[m] is video output.
  X: A to H (port)
  m: 0=lower bit, 1=higher bit
· Video output should be acquired at the rising timing of Pclk.
· Video output starts after the rising of Sync. Sync can be used as reference of data acquisition [refer to Timing chart (P.8)].
· On the rising edge of CTR, the lower bits are output from D0 and the higher bits from D6. CTR can be used as reference of data acquisition [refer to Timing chart (P.9)].

Current consumption

[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz, LR=125 klines/s]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vdd(A) terminal*10	Ic1	60	90	120	mA
Vdd(D) terminal*10	Ic2	170	280	390	
Vdd(C) terminal*10	Ic3	300	510	720	

*10: When saturation exposure light enters

Electrical characteristics of A/D converter [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz]

Parameter		Symbol	Specification	Unit
Resolution	High-speed mode	RESO	10*11	bit
	Low-speed mode		11*12	
Conversion voltage range		-	0 to 1.3	V

*11: Equivalent to 10-bit. From offset output to saturated output is approximately 1024 DN.
*12: Equivalent to 11-bit. From offset output to saturated output is approximately 2048 DN.

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz, gain: default value, offset: default value, tpi(MST)=8 μs (high-speed mode), 16 μs (low-speed mode)]

Common to all modes

Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ	400 to 1000			nm
Peak sensitivity wavelength		λp	-	700	-	nm
Photoresponse nonuniformity*13	Gain=1	PRNU	-	±5	±10	%
	Gain=8		-	±5	±10	
Image lag*14	Gain=1	Lag	-	-	0.1	%
Saturation charge		Qsat	96	100	-	ke^-
SNR max.	Gain=1	-	48	50	-	dB
	Gain=8		39	41	-	

*13: The output uniformity when a uniform light with a light exposure that is approximately 50% of saturation output is applied. It is defined as follows for the 2042 pixels excluding the 3 pixels at each end of the sensor.

$PRNU = (\Delta X/X) \times 100$ [%]

X: average output of all pixels, ΔX: difference between X and maximum output or minimum output

*14: The signal component of the previous data that remains after data is read out under saturation output conditions. Image lag increases if light greater than the saturation exposure is incident.

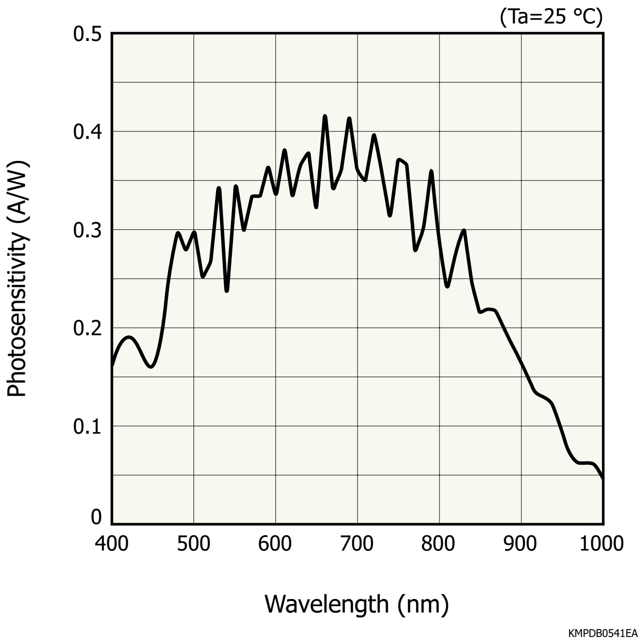
High-speed mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset variation*15	VSNU	1	-	2.5	15	mV
			-	2	12	DN
		8	-	8.8	53	mV
			-	7	42	DN
Dark output*16	VD	1	-	0.24	9.6	mV
			-	0.15	6	DN
		8	-	1.9	77	mV
			-	1.2	48	DN
Photosensitivity*17	Sw	1	-	54	-	V/(lx·s)
			-	43 k	-	DN/(lx·s)
		8	-	430	-	V/(lx·s)
			-	350 k	-	DN/(lx·s)
Conversion efficiency	CE	1	-	13	-	$\mu V/e^-$
			-	10	-	mDN/e^-
		8	-	100	-	$\mu V/e^-$
			-	80	-	mDN/e^-
Saturation output	Vsat	-	1.2	1.25	-	V
			975	1000	-	DN
Readout noise*18	Nread	1	-	0.63	1.9	mV-rms
			-	0.5	1.5	DN-rms
		8	-	1.2	3.4	mV-rms
			-	0.9	2.7	DN-rms
Dynamic range*19	Drange	1	650	2000	-	-
		8	460	1100	-	

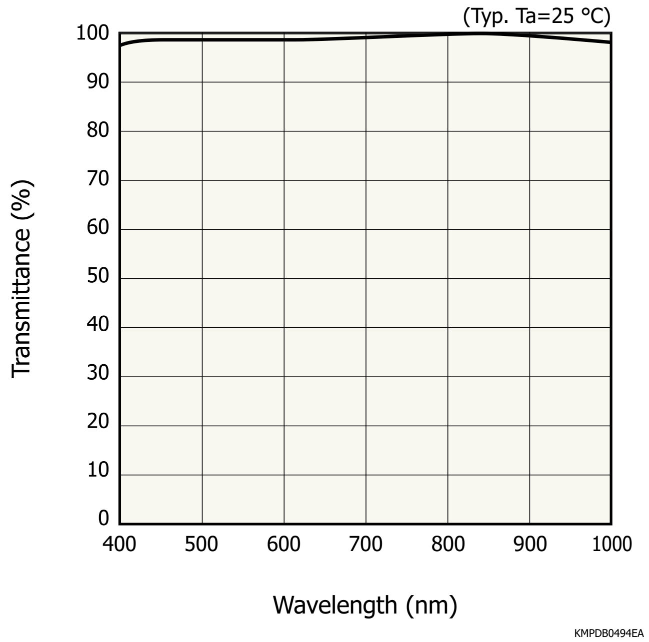
Low-speed mode						
Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset variation*15	VSNU	1	-	2.5	15	mV
			-	4	24	DN
		8	-	8.8	53	mV
			-	14	84	DN
Dark output*16	VD	1	-	0.24	9.6	mV
			-	0.3	12	DN
		8	-	1.9	77	mV
			-	2.4	96	DN
Photosensitivity*17	Sw	1	-	54	-	V/(lx·s)
			-	86 k	-	DN/(lx·s)
		8	-	430	-	V/(lx·s)
			-	690 k	-	DN/(lx·s)
Conversion efficiency	CE	1	-	13	-	μV/e-
			-	20	-	mDN/e-
		8	-	100	-	μV/e-
			-	160	-	mDN/e-
Saturation output	Vsat	-	1.2	1.25	-	V
			1950	2000	-	DN
Readout noise*18	Nread	1	-	0.44	1.3	mV-rms
			-	0.7	2.1	DN-rms
		8	-	1.1	3.2	mV-rms
			-	1.7	5.1	DN-rms
Dynamic range*19	Drange	1	930	2900	-	-
		8	380	1200	-	

*15: Measured in the dark state. Difference between the maximum and minimum.
*16: Ts=10 ms, voltage difference from the offset output level
*17: 2856 K, tungsten lamp
*18: Dark state
*19: Vsat/Nread
Note: DN (digital number): unit of A/D converter output

Spectral response (typical example)

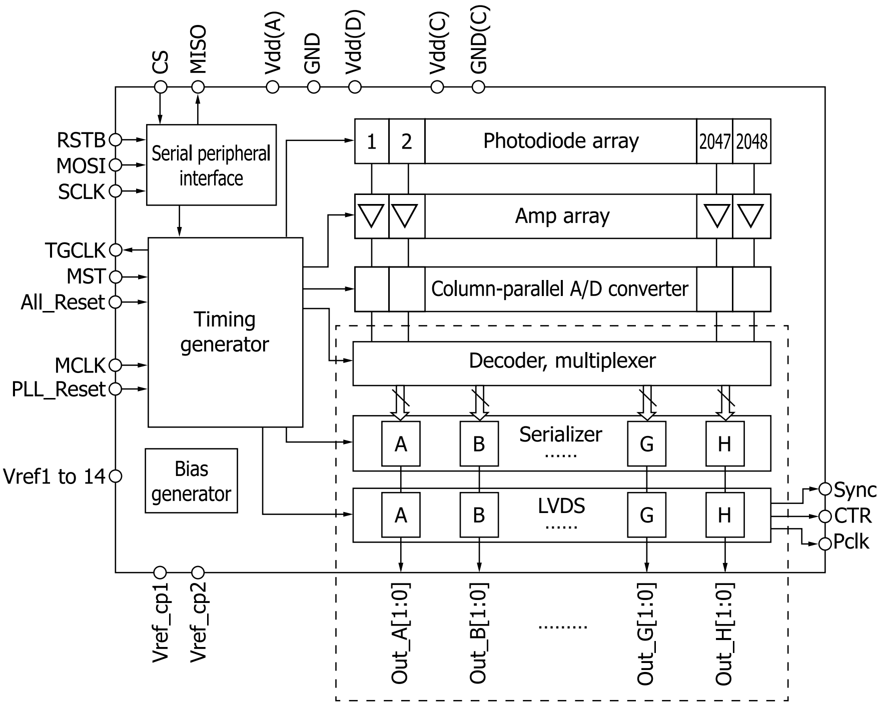


Spectral transmittance characteristics of window material



Block diagram

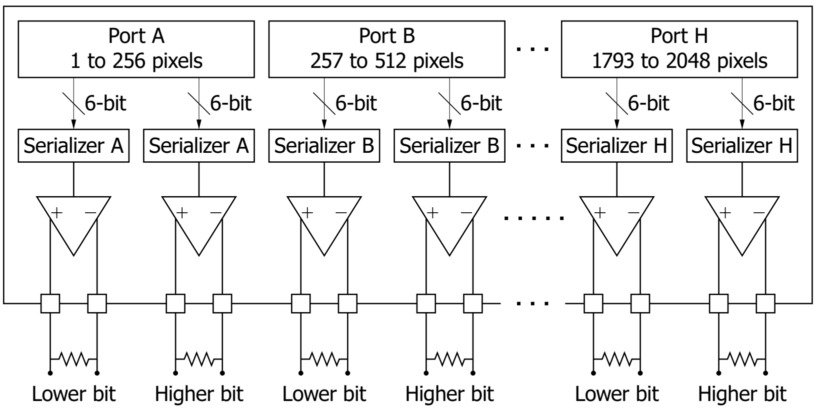
The video output signal is divided and output through 8 ports (A through H). Each port outputs 256 pixels of data (pixel numbers output from each port: A=1 to 256, B=257 to 512, ... H=1793 to 2048).



KMPDC0722EB

■ Enlarged view of video output (full output mode)

Output for each port divides data into LVDS (lower bits and higher bits) pairs.

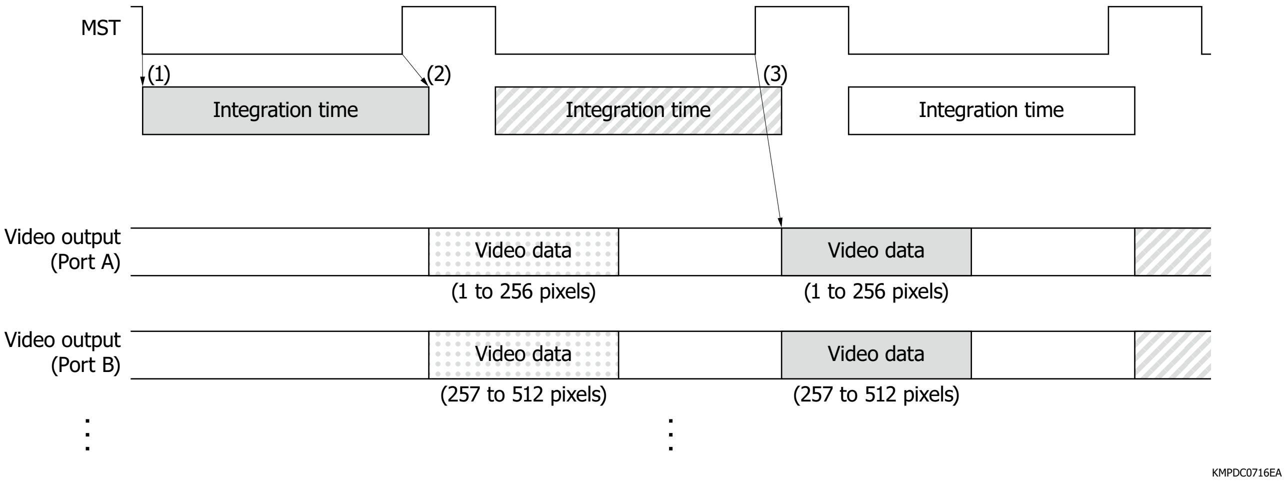


KMPDC0723EA

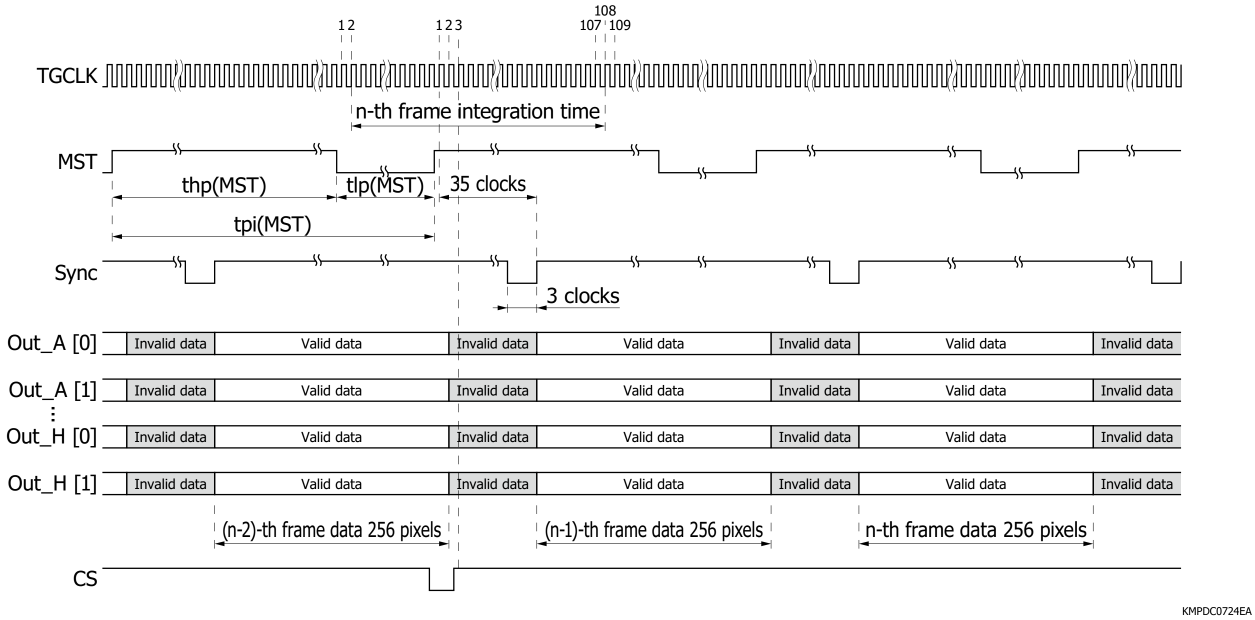
Timing chart

■ Description of operation

The integration time is determined by the low period of the start pulse.



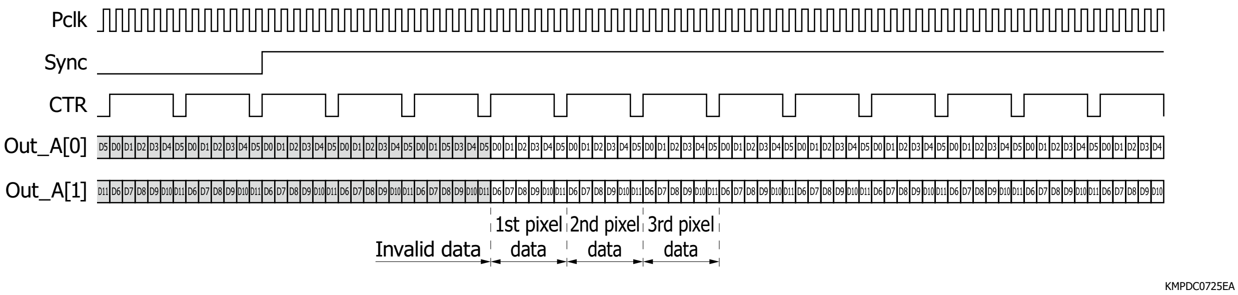
(1) The start of integration time is determined by the falling edge of the start pulse.
(2) The end of integration time is determined by the rising edge of the start pulse.
(3) Video data is output after the rising edge of the next start pulse cycle. Video data is output in order from the first pixel. (256 pixels of data are output for each port.)
* Signal integration is possible even during video output.



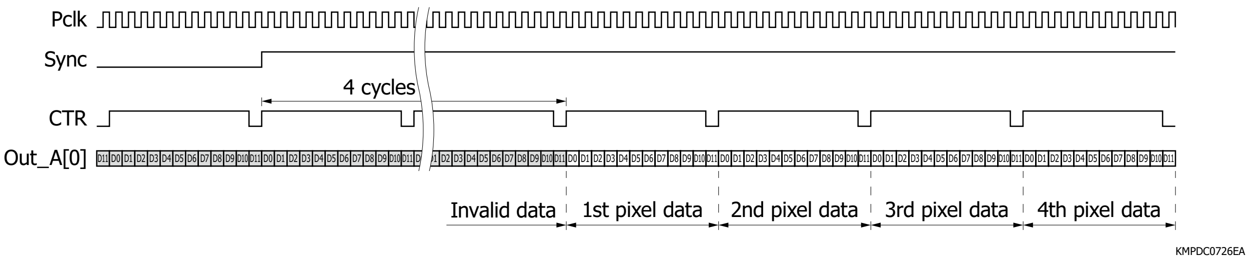
- Line rate equals the reciprocal of start pulse cycle.
- TGCLK is a timing generator clock inside the sensor. TGCLK is the same frequency as that of MCLK in high-speed mode, and the 1/2 in low-speed mode.
- The integration time equals the low period of start pulse plus 106 clock cycles of TGCLK.
- When the SPI register is set before the rising edge of the master start pulse plus 3 TGCLK, the SPI register setting is updated from the n-th frame data.
- In 1/2 output mode, only the following outputs are valid.
  Out_A[0], Out_B[0], Out_C[0], Out_D[0], Out_E[0], Out_F[0], Out_G[0] and Out_H[0]

Example: Port A

■ Full output mode



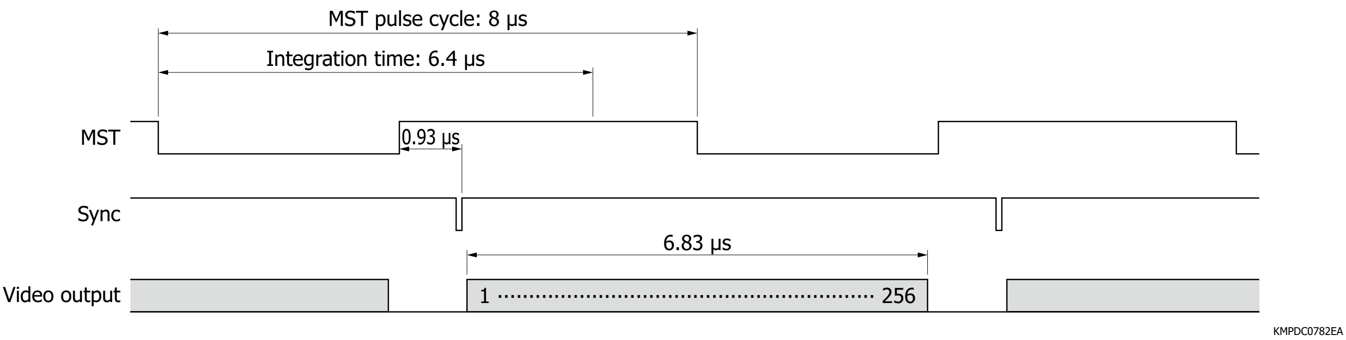
■ 1/2 output mode



Operation example

■ Example 1

Line rate=125 kline/s, master clock pulse frequency=37.5 MHz, high-speed mode, full output mode, integration time max.



· Master start pulse cycle = 300/f(MCLK) = 8 μs (equals the reciprocal of start pulse interval)

· Master start pulse's low period = Master start pulse cycle - Master start pulse's high period min.

= 300/f(MCLK) - 166/f(MCLK) = 300/37.5 MHz - 166/37.5 MHz = 134/37.5 MHz = 3.57 μs

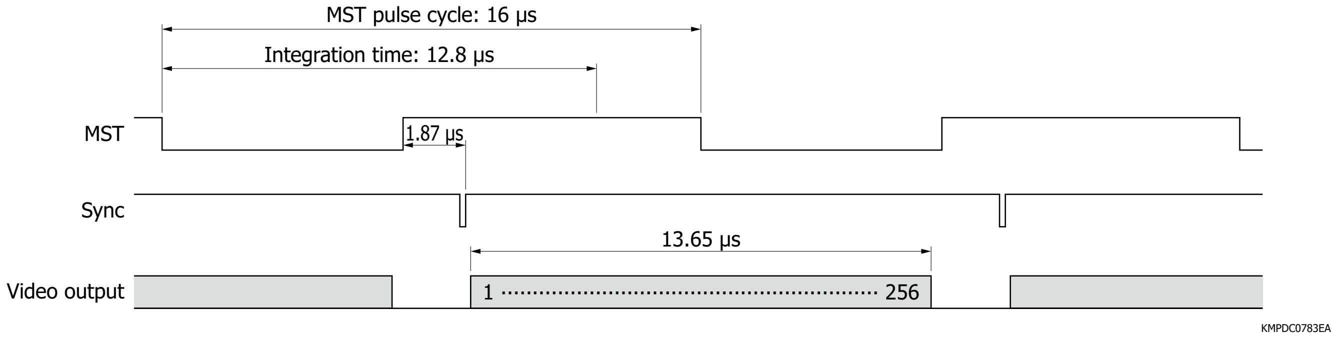
· Integration time = master start pulse low period + 106 cycles of master clock pulses

= (134 + 106)/37.5MHz = 6.4 μs

Sync rises about 0.93 μs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel (the signals from 256 pixels are output from each port).

■ Example 2:

Line rate=62.5kline/s, master clock pulse frequency=37.5MHz, low-speed mode, 1/2 output mode, integration time max.



· Master start pulse cycle = 600/f(MCLK) = 16 μs (equals the reciprocal of start pulse interval)

· Master start pulse's low period = Master start pulse cycle - Master start pulse's high period min.

= 600/f(MCLK) - 332/f(MCLK) = 600/37.5 MHz - 332/37.5 MHz = 268/37.5 MHz = 7.15 μs

· Integration time = Master start pulse low period + 212 cycles of master clock pulses

= (268 + 212)/37.5 MHz = 12.8 μs

Sync rises about 1.87 μs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel (the signals from 256 pixels are output from each port).

SPI address setting

Address (Decimal)	Register	Default value Binary	Default value Decimal	Setting
0	Mode[1:0]	---- --00	0	Mode[0] high-speed/low-speed mode (default: high-speed mode) Mode[1] number of video output terminal (default: full output mode)
19	Pclk_delay[5:0]	--00 0000	0	Pclk timing (default: Pclk_delay [5:0]=0)
20	AGC[4:0]	---1 0000	16	Gain (default: gain=1)
21	Offset[11:8]	---- 0000	31	Output offset (default: 31)
22	Offset[7:0]	0001 1111		

Note) Always set the addresses shown in the above table. The image sensor may malfunction if any other address is set.

High-speed/low-speed mode

Maximum line rate is selectable from following 2 modes:
It is set to High-speed mode when Mode[0] is 0 (Low), Low-speed mode when Mode[0] is 1 (High).
· High-speed mode (Mode[0]=0): Maximum line rate = 125 klines/s, A/D converter resolution = 10-bit
(From offset output to saturation output is approximately 1024 DN.)
· Low-speed mode (Mode[0]=1): Maximum line rate = 62.5 klines/s, A/D converter resolution = 11-bit
(From offset output to saturation output is approximately 2048 DN.)

Number of video output terminal

The number of video output terminal is selectable from following 2 modes [refer to the timing chart (P.9) in detail].
· Full output mode (Mode[1]=0): Video output=32 terminals (16 LVDS pairs)
· 1/2 output mode (Mode[1]=1): Video output=16 terminals (8 LVDS pairs)

Note: For the high-speed mode, do not set above setting.

Pclk timing

The Pclk output timing can be delayed inside the sensor. Set Pclk_delay[5:0] between 0 and 63.
When Pclk_delay[5:0] is increased by 1, the Pclk output is delayed by approximately 0.15 ns.

Gain setting

The sensor may not operate properly if a setting not in the following table is specified. Specify a setting shown in the table.

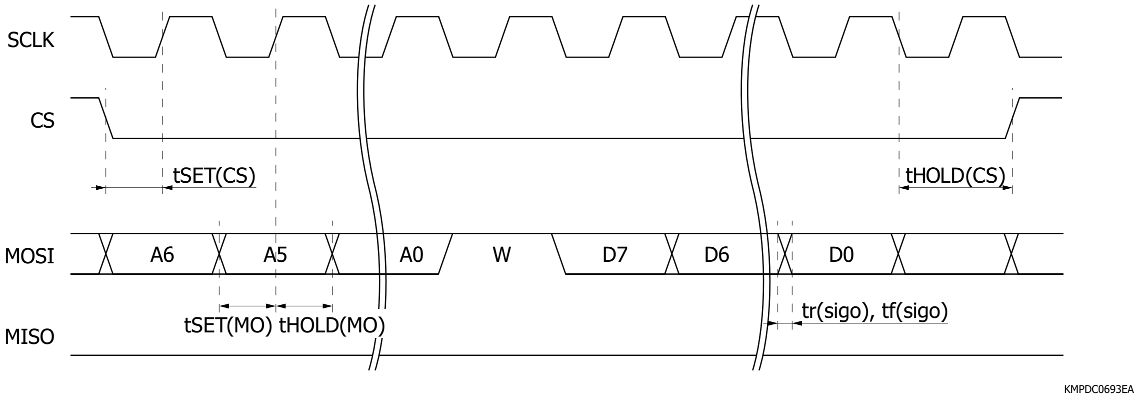
AGC[4:0]						Gain	Description
Decimal	Binary [4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	0	20	
1	0	0	0	0	1	10	
2	0	0	0	1	0	8	
4	0	0	1	0	0	4	
8	0	1	0	0	0	2	
16	1	0	0	0	0	1	Default setting

■ Output offset setting

Set Offset[11:0] between 0 and 1023. When Offset[11:0] is increased by 1, the offset value increases by 1 DN. Due to variations in individual differences of the product, the actual offset value will be slightly off from the specified value. Set offset[11:10] to 0.

SPI setting

Set the SPI using SCLK, CS, and MOSI. Setting RSTB to low level resets all parameters.



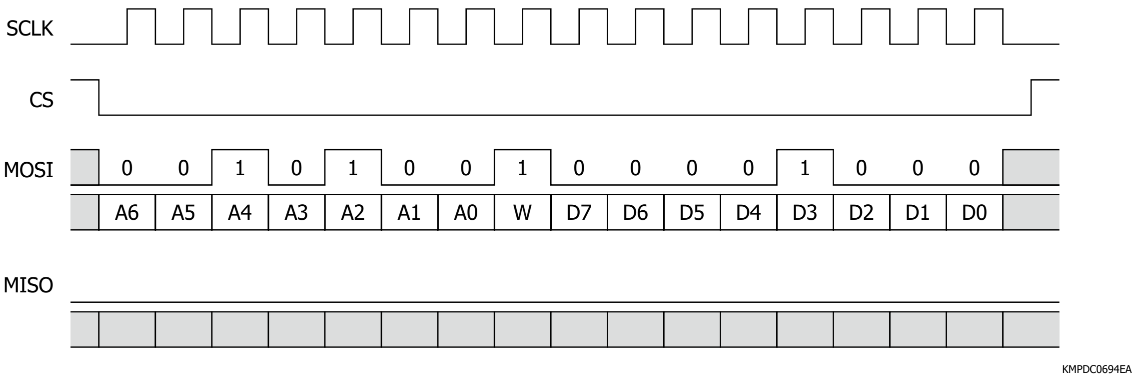
[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz, LR=125 klines/s]

Item	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	-	7.5	10	MHz
SPI setup time (CS)	tSET(CS)	7	-	-	ns
SPI hold time (CS)	tHOLD(CS)	7	-	-	ns
SPI setup time (MOSI)	tSET(MO)	7	-	-	ns
SPI hold time (MOSI)	tHOLD(MO)	7	-	-	ns
Digital input signal rise time*20	tr(sigi)	-	5	7	ns
Digital input signal fall time*20	tf(sigi)	-	5	7	ns

*20: The time for input voltage to rise or fall between 10% and 90%

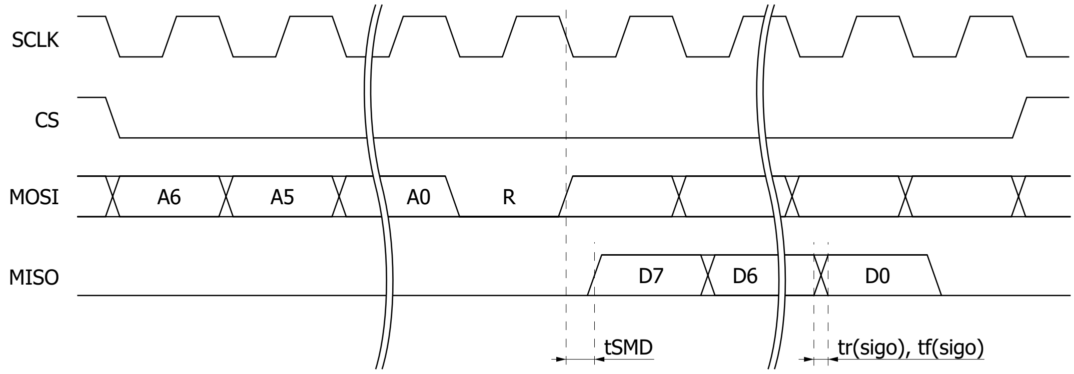
■ Example of SPI setting

Writing AGC [4:0]=8 (setting gain to 2 times)



Checking the SPI setting

You can check the current SPI setting in the following manner.



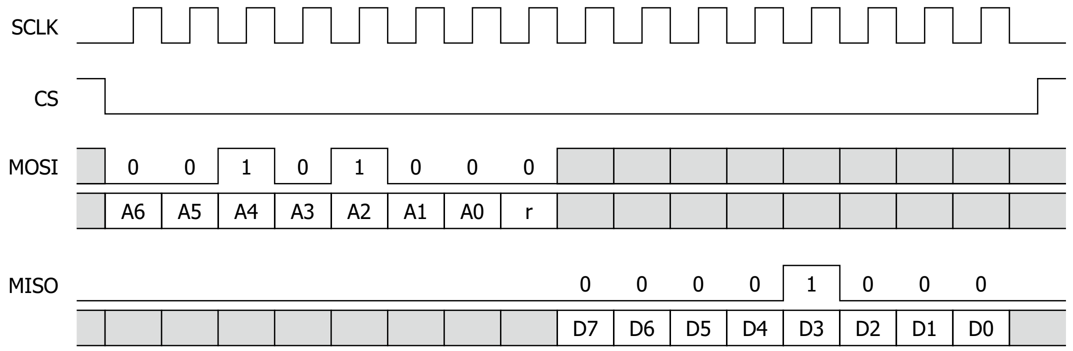
[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=37.5 MHz, LR=125 klines/s]

Item	Symbol	Min.	Typ.	Max.	Unit
Output signal rise time*21	tr(sigo)	-	10	12	ns
Output signal fall time*21	tf(sigo)	-	10	12	ns
SCLK-MISO output delay time	tSMD	-	-	25	ns

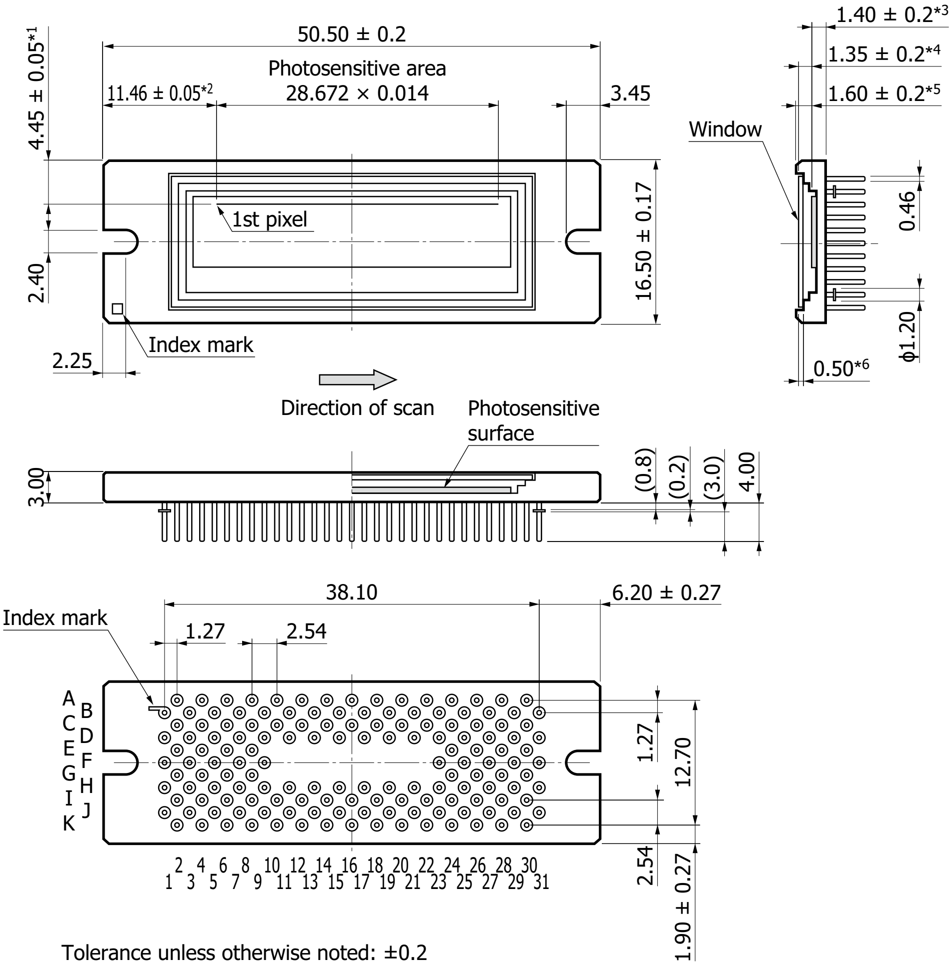
*21: Time for the output voltage to rise or fall between 10% and 90% when the load capacitance of the output terminal is 10 pF

■ Example of checking the SPI setting

Confirms AGC [4:0]=8 (gain=2 times)



Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
*1: Distance from package edge to photosensitive area center
*2: Distance from package edge to photosensitive area edge
*3: Distance from package bottom to photosensitive area
*4: Distance from glass surface to photosensitive surface
*5: Distance from package top to photosensitive surface
*6: Glass thickness

KMPDA0607EB

Pin connections

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
A2	Out_An[0]	Video output signal (LVDS)	O	D23	Vref6	Bias voltage*22	O
A4	Out_An[1]	Video output signal (LVDS)	O	D25	Syncp	Frame sync signal (LVDS)	O
A6	Out_Bn[0]	Video output signal (LVDS)	O	D27	MST	Master start signal (single end)	I
A8	Out_Bn[1]	Video output signal (LVDS)	O	D29	GND(C)	Ground	-
A10	Out_Cn[0]	Video output signal (LVDS)	O	D31	Vdd(C)	Supply voltage (3.3 V)	I
A12	Out_Cn[1]	Video output signal (LVDS)	O	E2	Vdd(D)	Supply voltage (3.3 V)	I
A14	Out_Dn[0]	Video output signal (LVDS)	O	E4	GND	Ground	-
A16	Out_Dn[1]	Video output signal (LVDS)	O	E6	PLL_reset	PLL circuit reset (single end)	I
A18	Out_En[0]	Video output signal (LVDS)	O	E8	CS	SPI selection signal (single end)	I
A20	Out_En[1]	Video output signal (LVDS)	O	E24	NC	No connection	-
A22	Out_Fn[0]	Video output signal (LVDS)	O	E26	All_reset	Timing generator reset (single end)	I
A24	Out_Fn[1]	Video output signal (LVDS)	O	E28	GND(C)	Ground	-
A26	Out_Gn[0]	Video output signal (LVDS)	O	E30	Vdd(C)	Supply voltage (3.3 V)	I
A28	Out_Gn[1]	Video output signal (LVDS)	O	F1	Vdd(D)	Supply voltage (3.3 V)	I
A30	Out_Hn[0]	Video output signal (LVDS)	O	F3	GND	Ground	-
B1	Out_Ap[0]	Video output signal (LVDS)	O	F5	SCLK	SPI clock signal (single end)	I
B3	Out_Ap[1]	Video output signal (LVDS)	O	F7	MOSI	SPI input signal (single end)	I
B5	Out_Bp[0]	Video output signal (LVDS)	O	F9	RSTB	SPI reset signal (single end)	I
B7	Out_Bp[1]	Video output signal (LVDS)	O	F23	NC	No connection	-
B9	Out_Cp[0]	Video output signal (LVDS)	O	F25	NC	No connection	-
B11	Out_Cp[1]	Video output signal (LVDS)	O	F27	NC	No connection	-
B13	Out_Dp[0]	Video output signal (LVDS)	O	F29	GND(C)	Ground	-
B15	Out_Dp[1]	Video output signal (LVDS)	O	F31	Vdd(C)	Supply voltage (3.3 V)	I
B17	Out_Ep[0]	Video output signal (LVDS)	O	G2	Vdd(D)	Supply voltage (3.3 V)	I
B19	Out_Ep[1]	Video output signal (LVDS)	O	G4	GND	Ground	-
B21	Out_Fp[0]	Video output signal (LVDS)	O	G6	MISO	SPI output signal (single end)	O
B23	Out_Fp[1]	Video output signal (LVDS)	O	G8	TGCLK	Timing generator clock signal (single end)	O
B25	Out_Gp[0]	Video output signal (LVDS)	O	G24	NC	No connection	-
B27	Out_Gp[1]	Video output signal (LVDS)	O	G26	NC	No connection	-
B29	Out_Hp[0]	Video output signal (LVDS)	O	G28	GND(C)	Ground	-
B31	Out_Hp[1]	Video output signal (LVDS)	O	G30	Vdd(C)	Supply voltage (3.3 V)	I
C2	Vdd(D)	Supply voltage (3.3 V)	I	H1	Vdd(D)	Supply voltage (3.3 V)	I
C4	GND	Ground	-	H3	GND	Ground	-
C6	Pclkn	Bit output sync signal (LVDS)	O	H5	NC	No connection	-
C8	CTRn	Pixel sync signal (LVDS)	O	H7	NC	No connection	-
C10	NC	No connection	-	H9	Vref7	Bias voltage*22	O
C12	NC	No connection	-	H11	Vref8	Bias voltage*22	O
C14	NC	No connection	-	H13	Vref9	Bias voltage*22	O
C16	NC	No connection	-	H15	Vref10	Bias voltage*22	O
C18	NC	No connection	-	H17	Vref11	Bias voltage*22	O
C20	NC	No connection	-	H19	Vref12	Bias voltage*22	O
C22	NC	No connection	-	H21	Vref13	Bias voltage*22	O
C24	NC	No connection	-	H23	Vref14	Bias voltage*22	O
C26	Syncn	Frame sync signal (LVDS)	O	H25	NC	No connection	-
C28	MCLK	Master clock signal (single end)	I	H27	NC	No connection	-
C30	Out_Hn[1]	Video output signal (LVDS)	O	H29	GND(C)	Ground	-
D1	Vdd(D)	Supply voltage (3.3 V)	I	H31	Vdd(C)	Supply voltage (3.3 V)	I
D3	GND	Ground	-	I2	Vdd(D)	Supply voltage (3.3 V)	I
D5	Pclkp	Bit output sync signal (LVDS)	O	I4	GND	Ground	-
D7	CTRp	Pixel sync signal (LVDS)	O	I6	NC	No connection	-
D9	Vref_cp1	Bias voltage for charge pump circuit (5.5 V)*22	O	I8	NC	No connection	-
D11	Vref_cp2	Bias voltage for charge pump circuit (-1.5 V)*22	O	I10	Vdd(A)	Supply voltage (3.3 V)	I
D13	Vref1	Bias voltage*22	O	I12	GND	Ground	-
D15	Vref2	Bias voltage*22	O	I14	Vdd(A)	Supply voltage (3.3 V)	I
D17	Vref3	Bias voltage*22	O	I16	GND	Ground	-
D19	Vref4	Bias voltage*22	O	I18	Vdd(A)	Supply voltage (3.3 V)	I
D21	Vref5	Bias voltage*22	O	I20	GND	Ground	-

*22: Insert a 1 µF capacitor between each terminal and GND.
Note: Leave NC pins open; do not connect to GND.

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
I22	Vdd(A)	Supply voltage (3.3 V)	I	J27	NC	No connection	-
I24	GND	Ground	-	J29	NC	No connection	-
I26	NC	No connection	-	J31	NC	No connection	-
I28	NC	No connection	-	K2	NC	No connection	-
I30	NC	No connection	-	K4	NC	No connection	-
J1	NC	No connection	-	K6	NC	No connection	-
J3	NC	No connection	-	K8	NC	No connection	-
J5	NC	No connection	-	K10	NC	No connection	-
J7	NC	No connection	-	K12	NC	No connection	-
J9	NC	No connection	-	K14	NC	No connection	-
J11	NC	No connection	-	K16	NC	No connection	-
J13	NC	No connection	-	K18	NC	No connection	-
J15	NC	No connection	-	K20	NC	No connection	-
J17	NC	No connection	-	K22	NC	No connection	-
J19	NC	No connection	-	K24	NC	No connection	-
J21	NC	No connection	-	K26	NC	No connection	-
J23	NC	No connection	-	K28	NC	No connection	-
J25	NC	No connection	-	K30	NC	No connection	-

Note: The video output symbol is defined as follows:

Out_An[0]

- [0]: lower (0 to 5) bits, [1]: higher (6 to 11) bits
- p: positive input of the differential pair, n: negative input of the differential pair
- A to H: output ports

Recommended soldering conditions

Parameter	Specification	Remarks
Solder temperature	260 °C max. (5 s or less)	

Note: When setting the soldering conditions, check for any problems by testing out the soldering methods in advance.

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window

If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

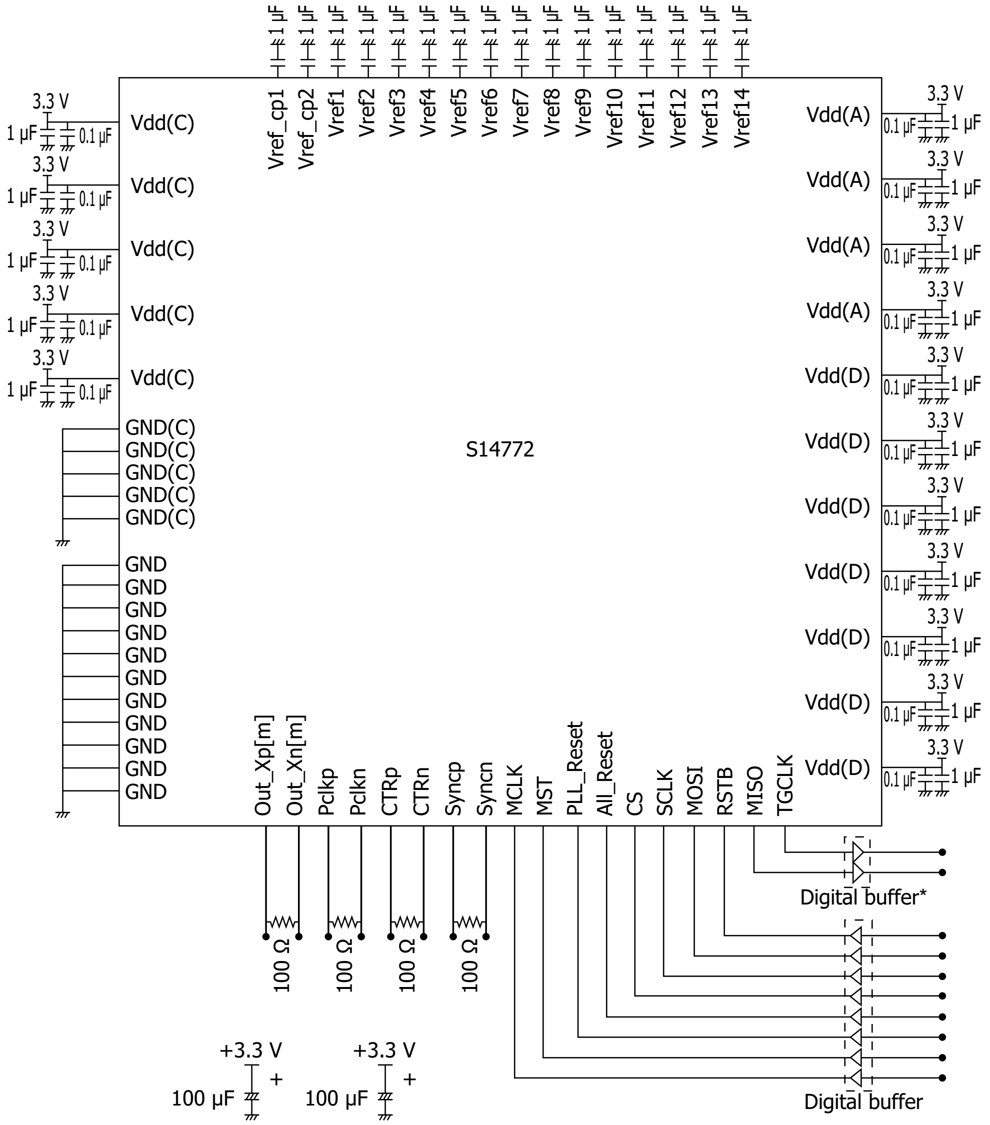
(3) UV light irradiation

Because this product is not designed to resist characteristic deterioration under UV light irradiation, do not apply UV light irradiation to it.

(4) Fixing the product in place

When using screws to fix the product in place, use M2 screws. Set the tightening torque to 0.08 N·m or less.

Connection circuit example



Connect GND and GND(C) with a single point.
* Digital buffer is not necessary if MISO or TGCLK is not used.

KMPDC0727EA

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical note
· CMOS linear image sensors

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www.hamamatsu.com

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184
U.S.A.: HAMAMATSU CORPORATION: 360 Foothill Road, Bridgewater, NJ 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218 E-mail: usa@hamamatsu.com
Germany: HAMAMATSU PHOTONICS DEUTSCHLAND GMBH.: Arzbergerstr. 10, 82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8 E-mail: info@hamamatsu.de
France: HAMAMATSU PHOTONICS FRANCE S.A.R.L.: 19 Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10 E-mail: infos@hamamatsu.fr
United Kingdom: HAMAMATSU PHOTONICS UK LIMITED: 2 Howard Court,10 Tewin Road, Welwyn Garden City, Hertfordshire, AL7 1BW, UK, Telephone: (44)1707-294888, Fax: (44)1707-325777 E-mail: info@hamamatsu.co.uk
North Europe: HAMAMATSU PHOTONICS NORDEN AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46)8-509 031 00, Fax: (46)8-509 031 01 E-mail: info@hamamatsu.se
Italy: HAMAMATSU PHOTONICS ITALIA S.R.L.: Strada della Moia, 1 int. 6, 20044 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41 E-mail: info@hamamatsu.it
China: HAMAMATSU PHOTONICS (CHINA) CO., LTD.: 1201 Tower B, Jiaming Center, 27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R. China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866 E-mail: hpc@hamamatsu.com.cn
Taiwan: HAMAMATSU PHOTONICS TAIWAN CO., LTD.: 8F-3, No.158, Section 2, Gongdao 5th Road, East District, Hsinchu, 300, Taiwan R.O.C. Telephone: (886)3-659-0080, Fax: (886)3-659-0081 E-mail: info@hamamatsu.com.tw

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