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TDI-CCD area image sensor

S7199-01/-01F

Image sensor with a long, narrow photosensitive area for X-ray imaging

The S7199-01 is a front-illuminated FFT-CCD image sensor developed for X-ray imaging. An FOS (Fiber Optic plate with Scintillator) sensitive to X-rays is directly coupled to the CCD chips, allowing X-ray imaging with high sensitivity. Two CCD chips are arranged in close proximity to configure a long photosensitive area (approx. 150 mm).
The S7199-01 CCD image sensor features TDI mode operation that allows capturing clear, sharp X-ray images of objects moving on a belt conveyor, making it ideal for non-destructive X-ray inspection. FOP type not coated with scintillator material is also provided (S7199-01F).

Features

- **1536 × 128 pixel (× 2 chips)**
- **Pixel size: 48 × 48 µm**
- **Buttable structure of 2 chips**
- **TDI (time delay integration) operation**
- **100% fill factor**
- **Wide dynamic range**
- **Low dark current**
- **Low readout noise**
- **MPP operation**

Applications

- **General X-ray imaging**
- **Non-destructive inspection**
- **Dental panorama**

Specifications

Parameter	S7199-01	S7199-01F
CCD structure	Full frame transfer or TDI	
Window	FOS (fiber optic plate with scintillator)	FOP (fiber optic plate)*1
Photosensitive area (H × V)	73.728 × 6.144 mm (× 2 chips)	
X-ray sensitive area	146 × 6 mm	-
Pixel size (H × V)	48 × 48 µm	
Number of total pixels (H × V)	1536 × 128 (× 2 chips)	
Number of effective pixels (H × V)	1536 × 128 (× 2 chips)	
Fill factor	100%	
Vertical clock phase	2 phases	
Horizontal clock phase	2 phases	
Output circuit	Two-stage MOSFET source follower with load resistance	
X-ray resolution	4 to 6 Lp/mm at 60 kVp, 20 µGy	-
Total dose irradiation	50 Gy max.	-
Package	40-pin ceramic	
Cooling	Non-cooled	

*1: When using this product for X-ray detection, the user needs to affix a phosphor sheet, etc. to the FOP.

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	-20	-	+70	°C
Operating temperature	Topr	0	-	+40	°C
OD voltage	V_{OD}	-0.5	-	+20	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
IGV voltage	V_{IGV}	-15	-	+15	V
IGH voltage	V_{IGH}	-15	-	+15	V
SG voltage	V_{SG}	-15	-	+15	V
OG voltage	V_{OG}	-15	-	+15	V
RG voltage	V_{RG}	-15	-	+15	V
TG voltage	V_{TG}	-15	-	+15	V
Vertical clock voltage	V_{P1AV}, V_{P2AV} V_{P1BV}, V_{P2BV}	-15	-	+15	V
Horizontal clock voltage	V_{P1AH}, V_{P2AH} V_{P1BH}, V_{P2BH}	-15	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	12	15	-	V
Reset drain voltage		V_{RD}	12	13	14	V
Output gate voltage		V_{OG}	-0.5	2	5	V
Output transistor ground voltage		V_{SSA}	-	0	-	V
Substrate voltage		V_{SSD}	-5	0	-	V
Test point	Vertical input source	V_{ISV}	-	V_{RD}	-	V
	Vertical input gate	V_{IGV}	-8	0	-	
	Horizontal input gate	V_{IGH}	-8	0	-	
Vertical shift register clock voltage	High	V_{P1AVH}, V_{P2AVH} V_{P1BVH}, V_{P2BVH}	0	3	6	V
	Low	V_{P1AVL}, V_{P2AVL} V_{P1BVL}, V_{P2BVL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1AHH}, V_{P2AHH} V_{P1BHH}, V_{P2BHH}	0	3	6	V
	Low	V_{P1AHL}, V_{P2AHL} V_{P1BHL}, V_{P2BHL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	0	3	6	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	0	3	6	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	0	3	6	V
	Low	V_{TGL}	-9	-8	-7	

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	C_{P1AV}, C_{P2AV} C_{P1BV}, C_{P2BV}		-	15000	-	pF
Horizontal shift register capacitance	C_{P1AH}, C_{P2AH} C_{P1BH}, C_{P2BH}		-	500	-	pF
Summing gate capacitance	C_{SG}		-	15	-	pF
Reset gate capacitance	C_{RG}		-	10	-	pF
Transfer gate capacitance	C_{TG}		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	-
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3 *4	-	60	-	mW

*2: Measured at half of the full well capacity. CTE is defined per pixel.
*3: V_{OD}=15 V
*4: Power dissipation of the on-chip amplifier (each chip)

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat		-	Fw × Sv	-	V
Full well capacity		Vertical	Fw		600	1200	-	ke^-
		Horizontal			600	1200	-	
		Summing			600	1200	-	
CCD node sensitivity			Sv	*5	0.45	0.6	-	$\mu V/e^-$
Dark current (MPP mode)			DS	*6	-	8	24	ke^-/pixel/s
Readout noise		Ta=25 °C	Nr	*7	-	90	-	e^- rms
		Ta=-40 °C			-	60	120	
Dynamic range			DR	*8	5000	20000	-	
X-ray response nonuniformity (S7199-01)			XRNU	*9	-	±10	±30	%
Photoresponse nonuniformity (S7199-01F)			PRNU	*10				
Blemish	Point defects*11	White spots	-		-	-	10	-
		Black spots			-	-	10	
	Cluster defects			*12	-	-	0	
	Column defects			*13	-	-	0	
X-ray resolution (S7199-01)			ΔR		4	6	-	Lp/mm

*5: V_{OD}=15 V
*6: Dark current doubles for every 5 to 7 °C.
*7: Operating frequency is 2 MHz.
*8: Dynamic range = Full well capacity / Readout noise
*9: X-ray irradiation of 60kVp, measured at half of the full well capacity.
Measuring region that is within 146.0 mm (H) × 6.0 mm (V) (refer to dimensional outline)

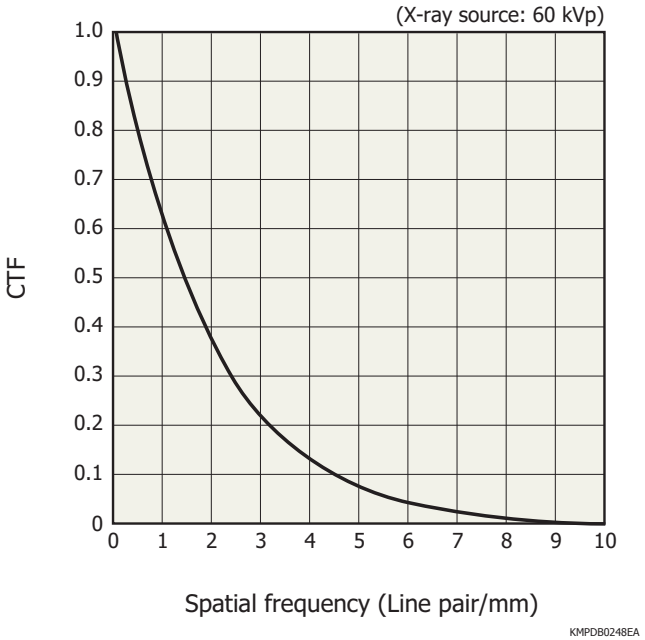
$$\text{XRNU [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 565 nm)

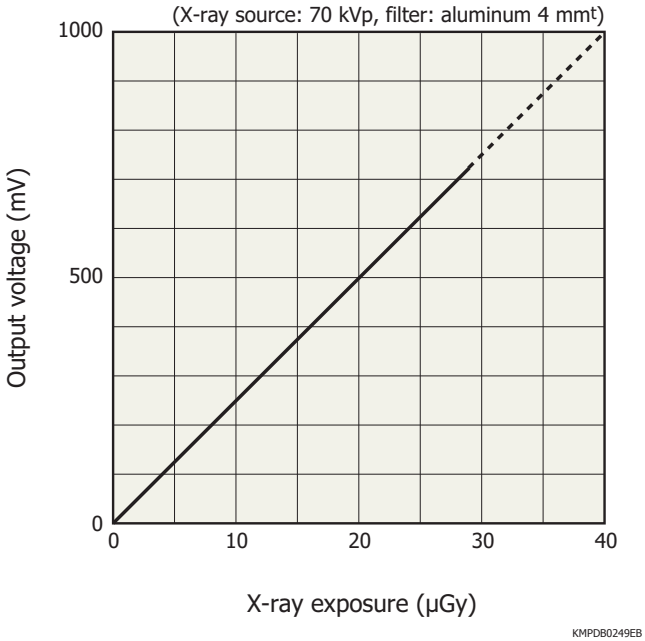
$$\text{PRNU [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*11: White spots > 20 times of typ. dark signal (8 ke^-/pixel/s)
Black spots > 50% reduction in response relative to adjacent pixels, measured at half of the full well capacity
*12: Continuous 2 to 9 point defects
*13: Continuous >10 point defects

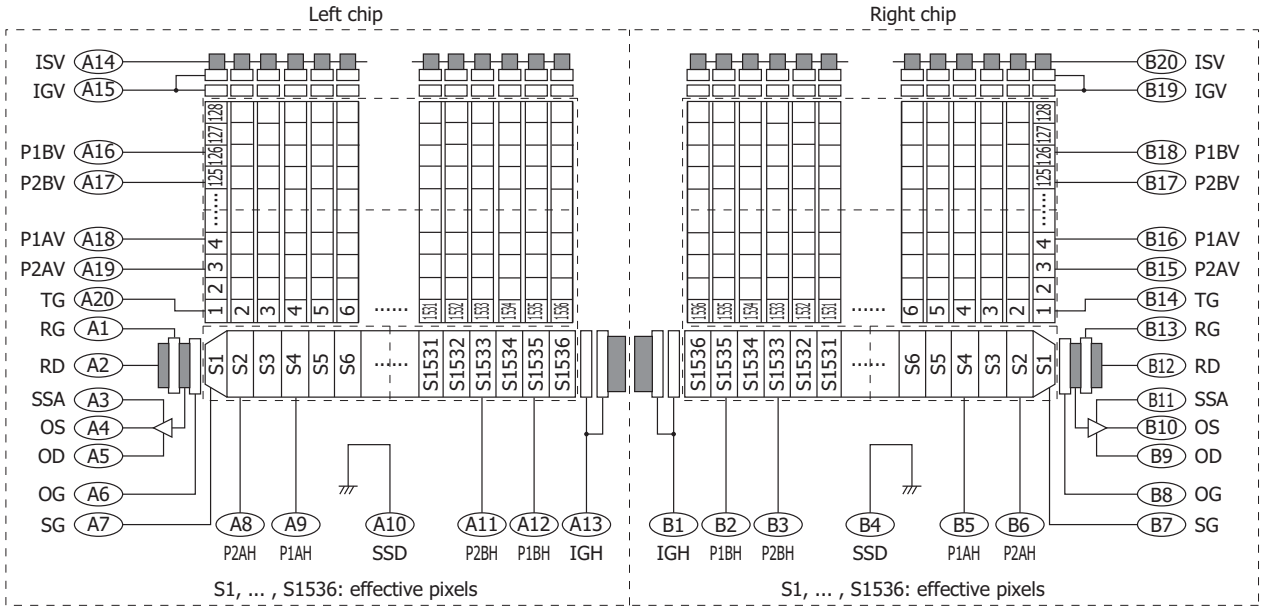
Resolution (S7199-01)



Output voltage vs. X-ray response (S7199-01)



Device structure

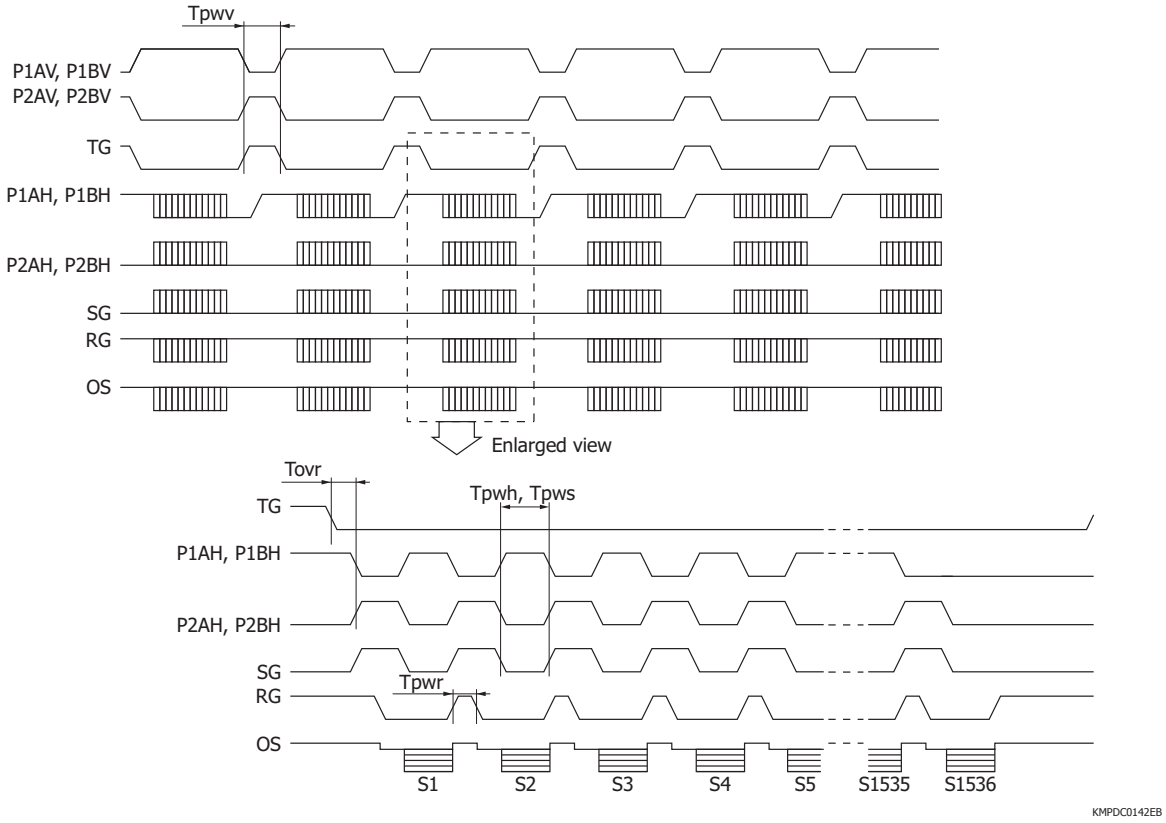


Pixel format

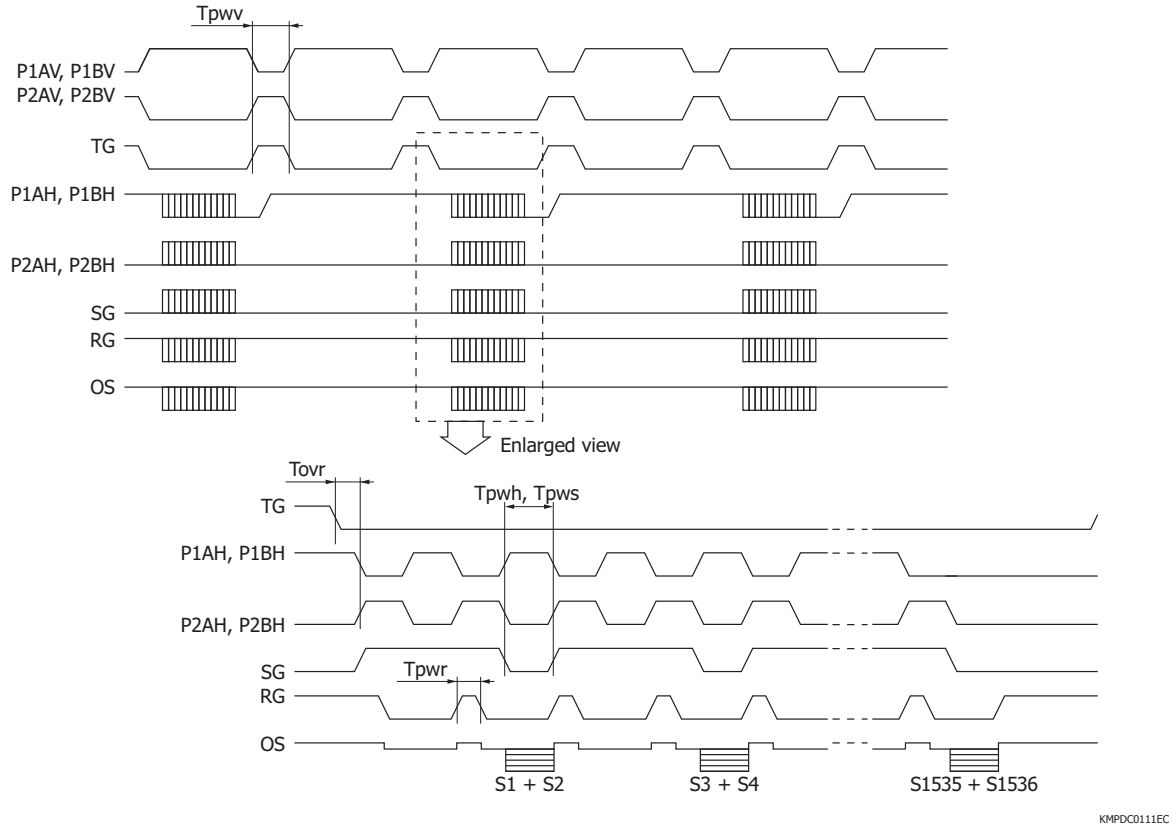
← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
0	128	0

Timing chart (TDI operation)



Timing chart (TDI operation, 2 × 2 pixel binning)

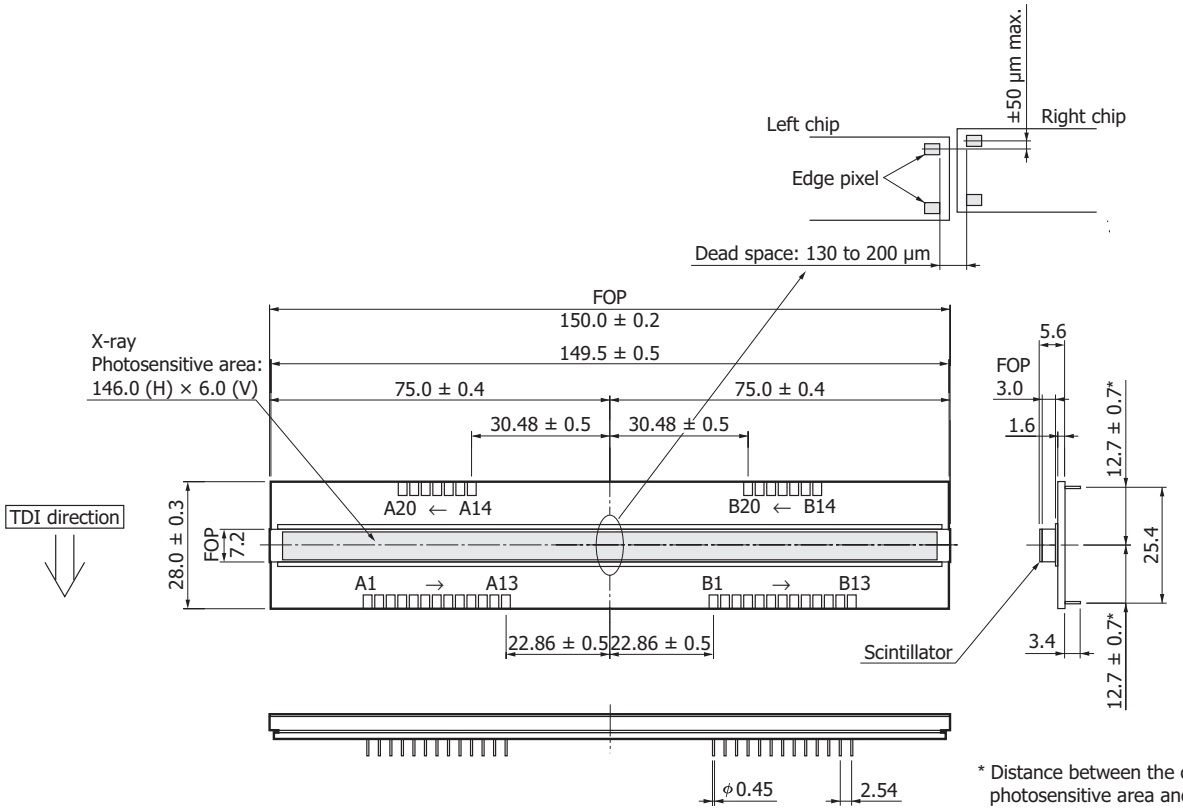


Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1AV, P1BV, P2AV, P2BV, TG	Pulse width	tpwv	*14 *15	30	60	-	µs
	Rise and fall times	tprv, tpfv		200	-	-	ns
P1AH, P1BH, P2AH, P2BH	Pulse width	tpwh	*15	125	250	-	ns
	Rise and fall times	tprh, tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	tpws		125	250	-	ns
	Rise and fall times	tprs, tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	tpwr		10	50	-	ns
	Rise and fall times	tprr, tpfr		5	-	-	ns
TG-P1AH, P1BH	Overlap time	tovr		10	20	-	µs

*14: TG terminal can be short-circuited to P2AV terminal.
*15: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

S7199-01



* Distance between the center of photosensitive area and the I/O pins

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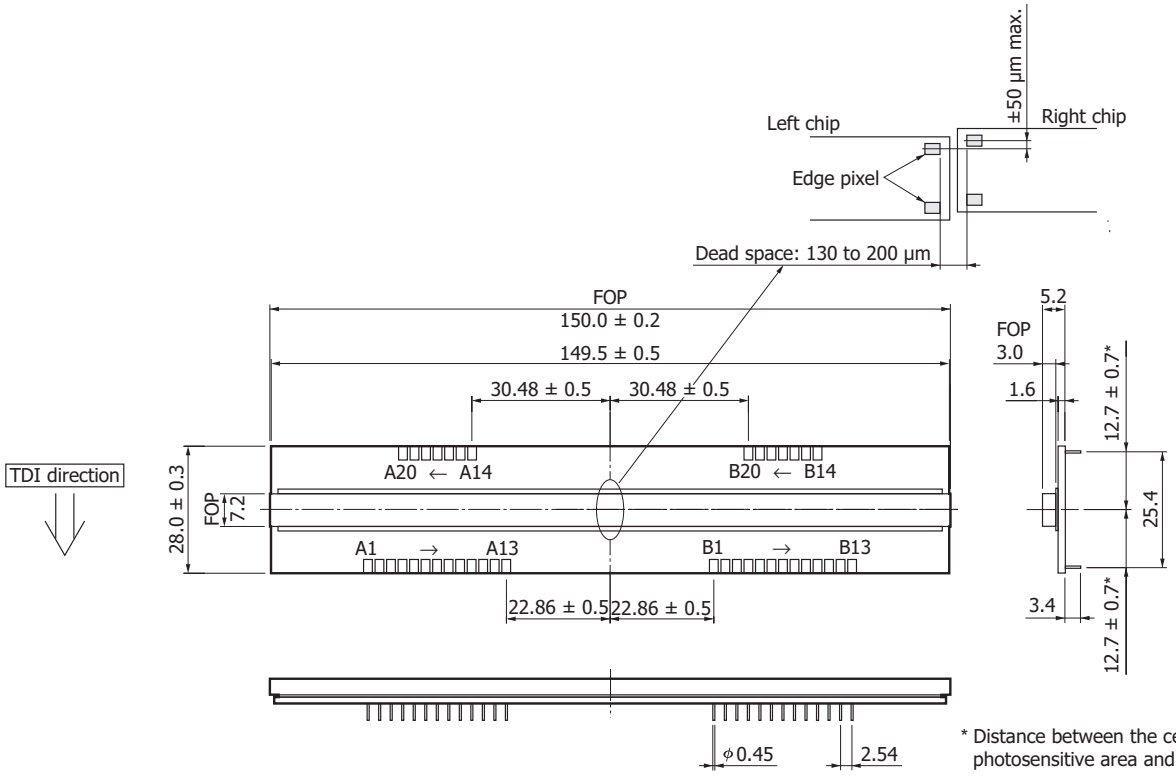
S7199-01F



* Distance between the center of photosensitive area and the I/O pins

KMPDA0282EC

Pin connections

Pin no.	Symbol	Description	Remark
A1	RG	Reset gate	
A2	RD	Reset drain	
A3	SSA	Analog ground	
A4	OS	Output transistor source	
A5	OD	Output transistor drain	
A6	OG	Output gate	
A7	SG	Summing gate	
A8	P2AH	CCD horizontal register clock A-2	
A9	P1AH	CCD horizontal register clock A-1	
A10	SSD	Digital ground	
A11	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
A12	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
A13	IGH	Test point (horizontal input gate)	
A14	ISV	Test point (vertical input source)	Shorted to RD
A15	IGV	Test point (vertical input gate)	
A16	P1BV	CCD vertical register clock B-1	Same timing as P1AV
A17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
A18	P1AV	CCD vertical register clock A-1	
A19	P2AV	CCD vertical register clock A-2	
A20	TG	Transfer gate	
B1	IGH	Test point (horizontal input gate)	
B2	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
B3	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
B4	SSD	Digital ground	
B5	P1AH	CCD horizontal register clock A-1	
B6	P2AH	CCD horizontal register clock A-2	
B7	SG	Summing gate	
B8	OG	Output gate	
B9	OD	Output transistor drain	
B10	OS	Output transistor source	
B11	SSA	Analog ground	
B12	RD	Reset drain	
B13	RG	Reset gate	
B14	TG	Transfer gate	
B15	P2AV	CCD vertical register clock A-2	
B16	P1AV	CCD vertical register clock A-1	
B17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
B18	P1BV	CCD vertical register clock B-1	Same timing as P1AV
B19	IGV	Test point (vertical input gate)	
B20	ISV	Test Point (vertical input source)	Shorted to RD

Precautions (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use an anti-static wrist band, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Take these measures as needed to prevent electrostatic damage to the sensor.

Notice

- This product is warranted for a period of 12 months after the date of the shipment.
  The warranty is limited to replacement or repair of any defective product due to defects in workmanship or materials used in manufacture. The warranty does not cover loss or damage caused by natural disaster, misuse (including modifications and any use not complying with the environment, application, usage and storage conditions described in this datasheet), or total radiation dose over 50 Gy (incident X-ray energy: 70 kVp) even within the warranty period.

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